GPU Programming

Introduction and Historical Notes

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A Perspective

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- In 1958 parallel computing was introduced by S. Gill introducing *branching and waiting*, while at IBM J. Cocke and D. Slotnick discussed *parallelism in numerical calculations*

- The D825 by Burroughs Corporation, introduced n 1962, was the first *modern* parallel computer with four-processors

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- Things changed greatly in the 1990s

S3 Virge

My first graphics card (1991)

The World is 3D

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- Now we know them by the term “GPUs” (thanks to Nvidia’s marketing team)

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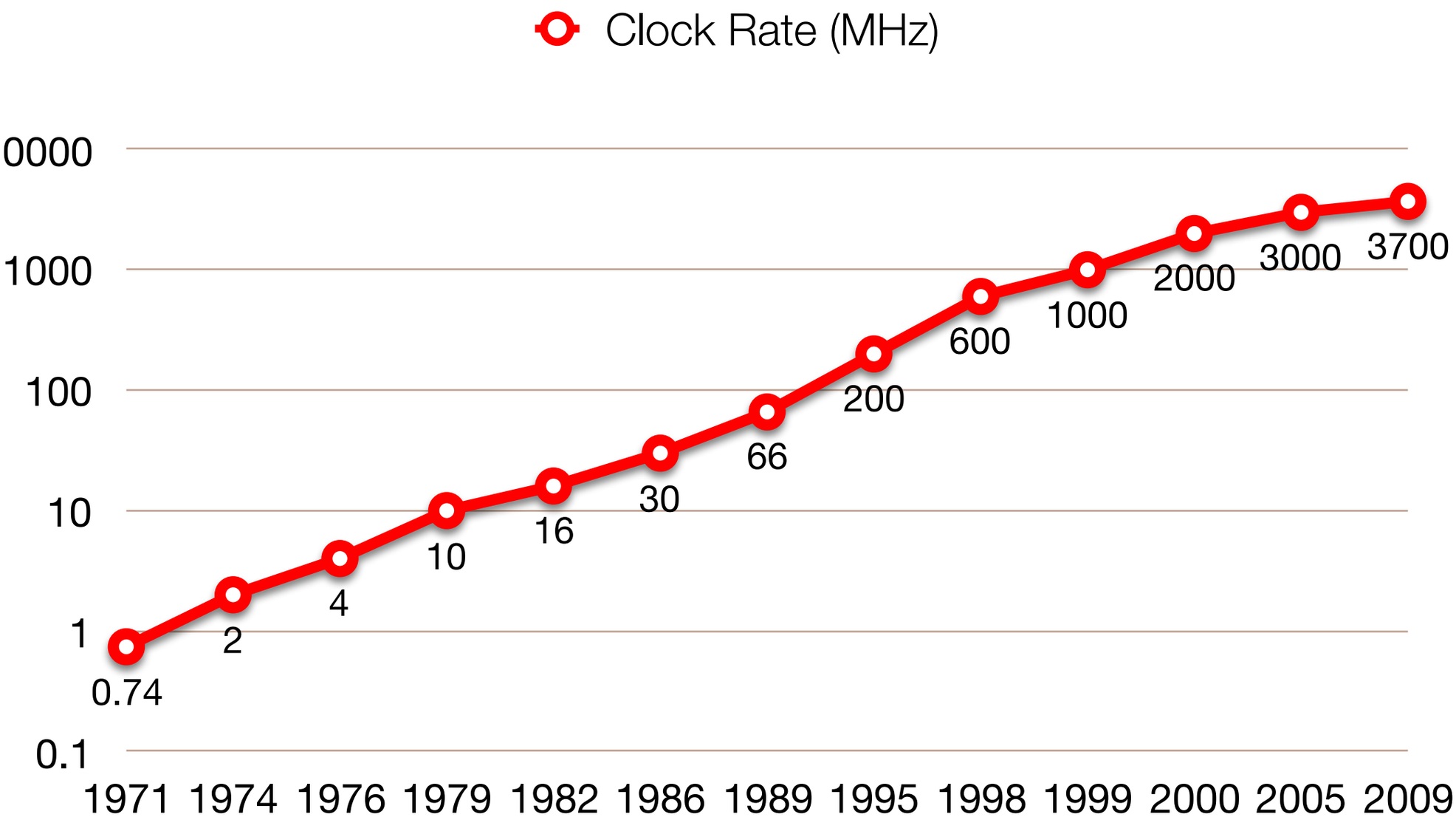
- The trend is obviously rising for GPUs, flat for CPUs

CPU Clock Rate



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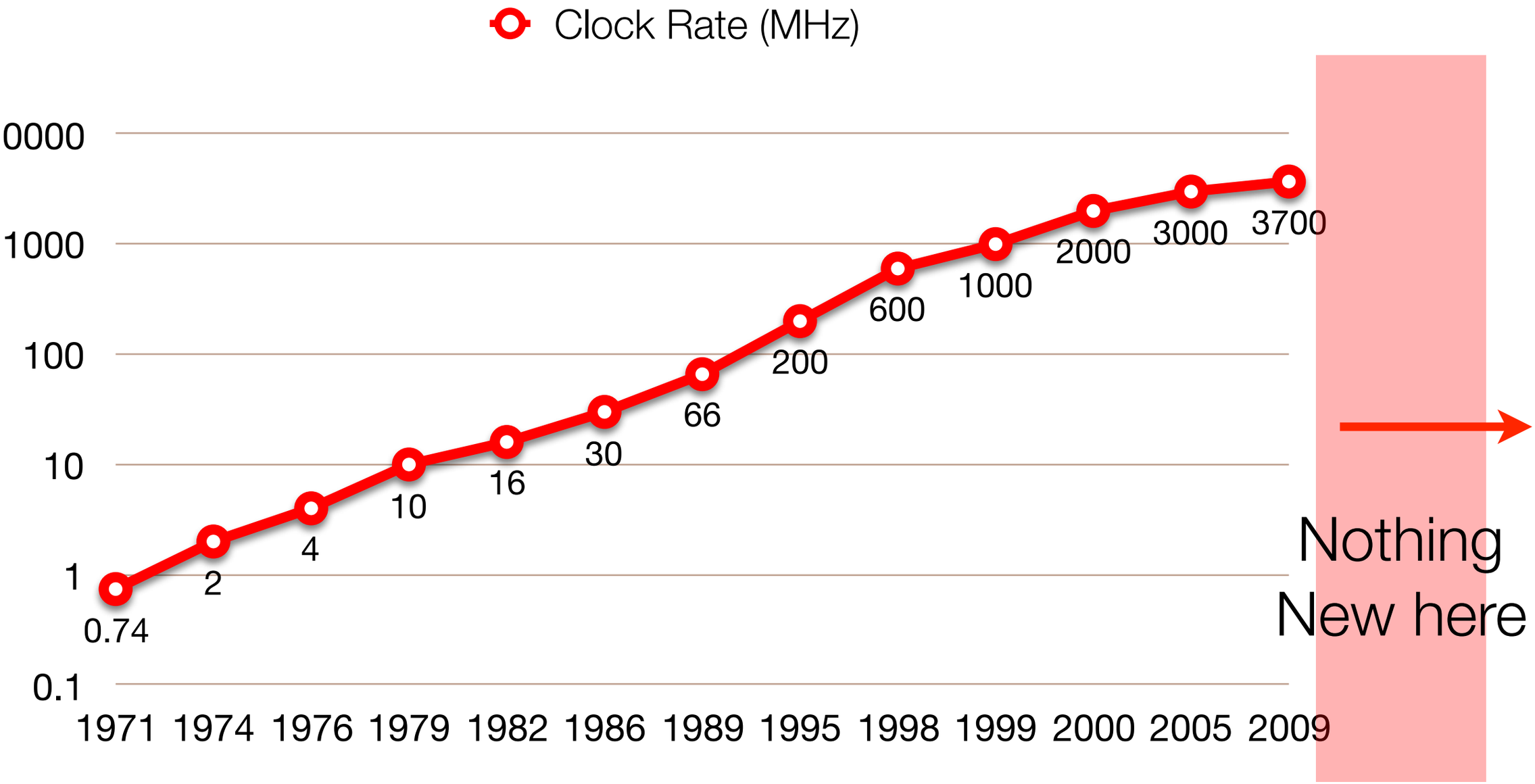

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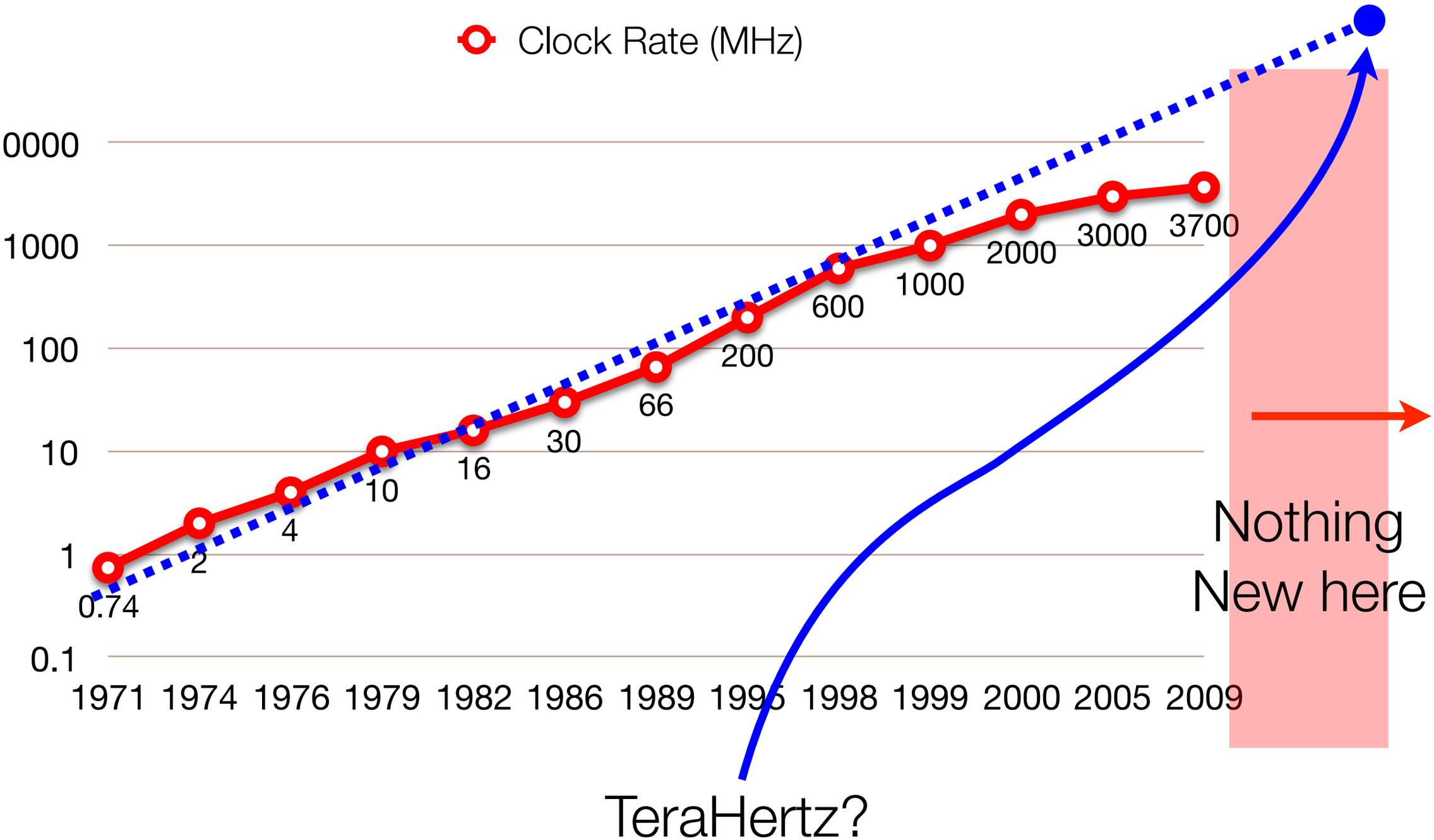
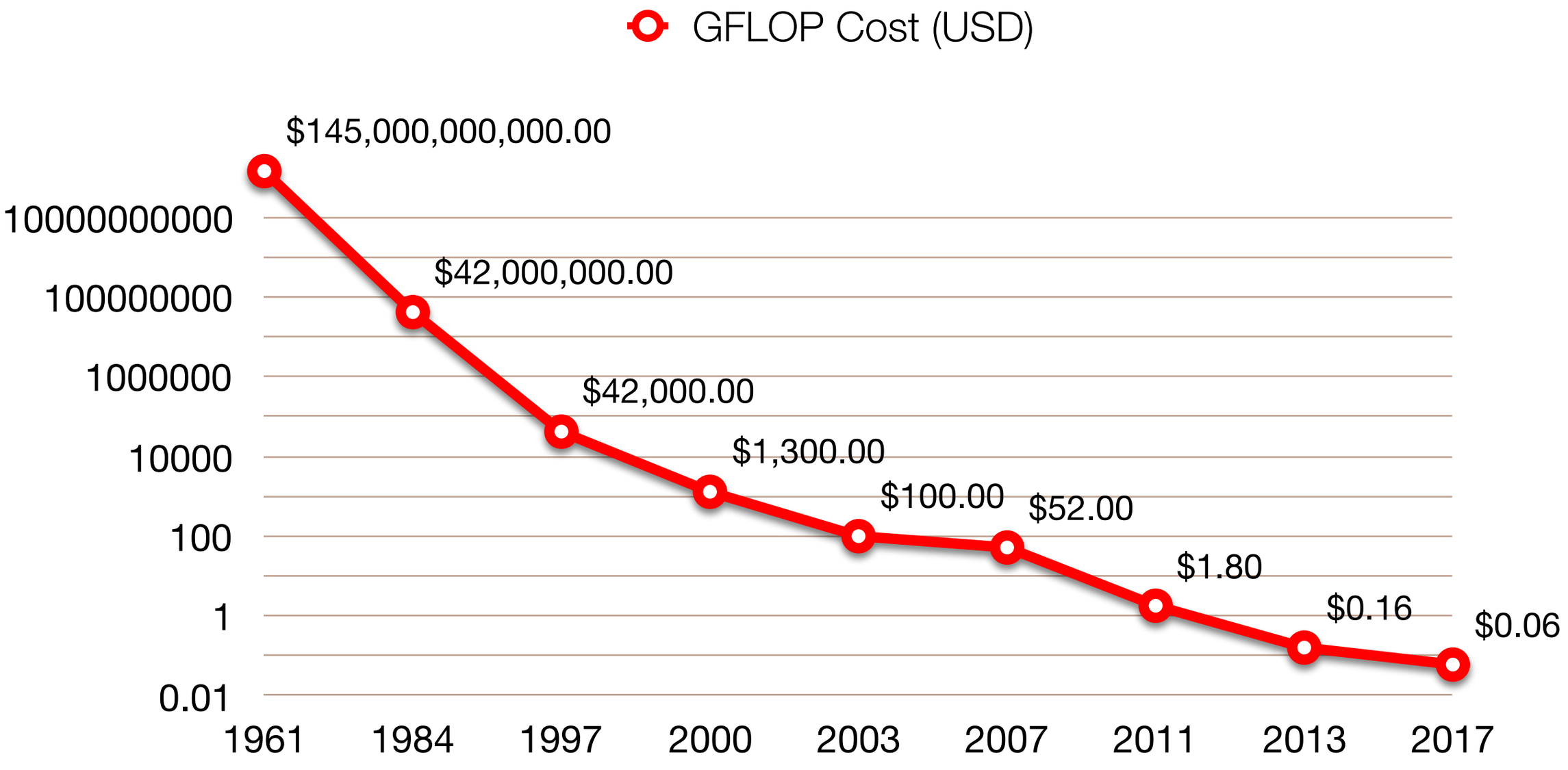
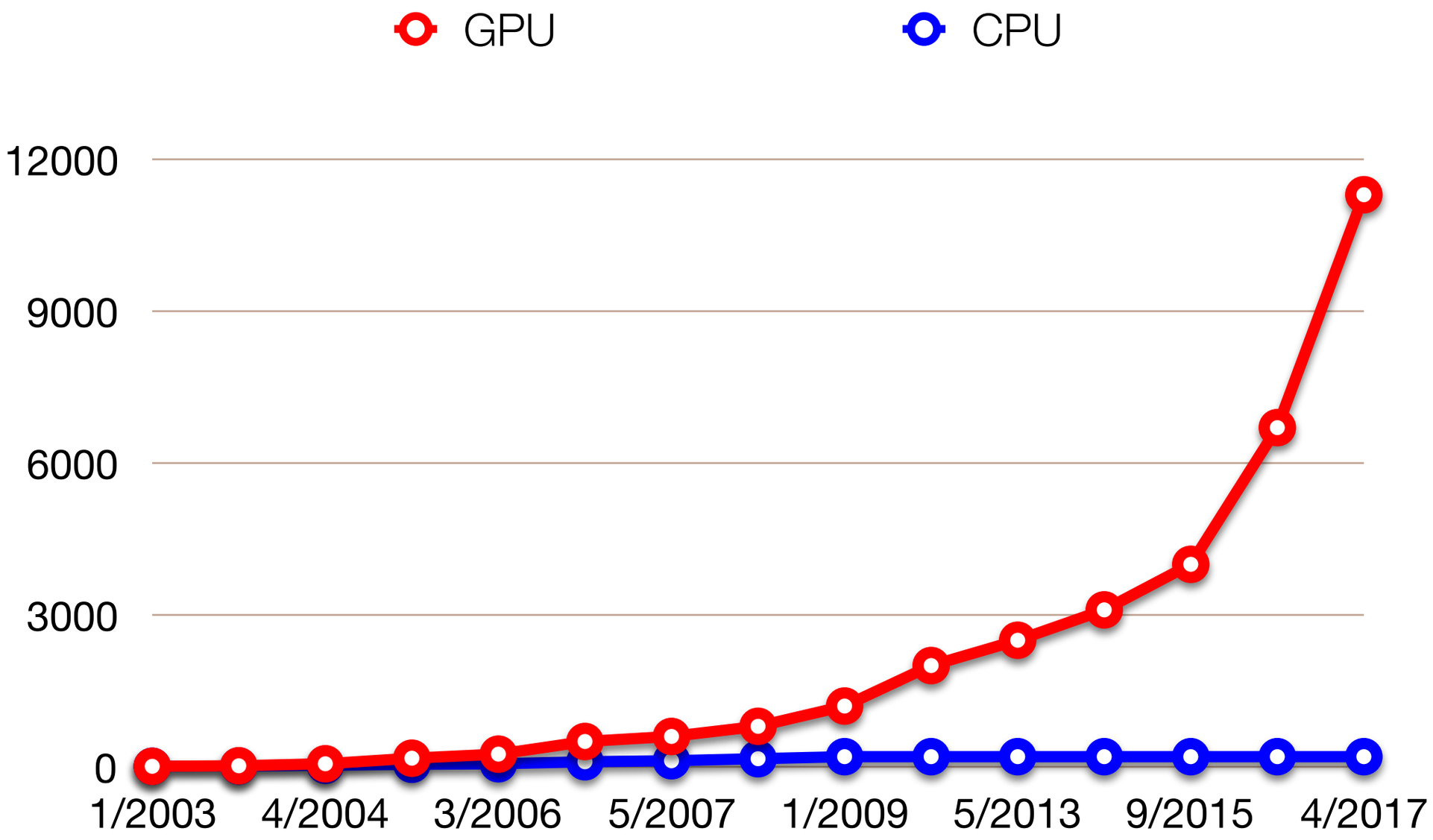


Cost of Performances



GFLOPs


GPU
CPU
12000
9000
6000
3000
0
1/2003
4/2004
3/2006
5/2007
1/2009
5/2013
9/2015
4/2017

Who uses GPUs?

TL;DR:
everyone, even if you don’t know

Speedup

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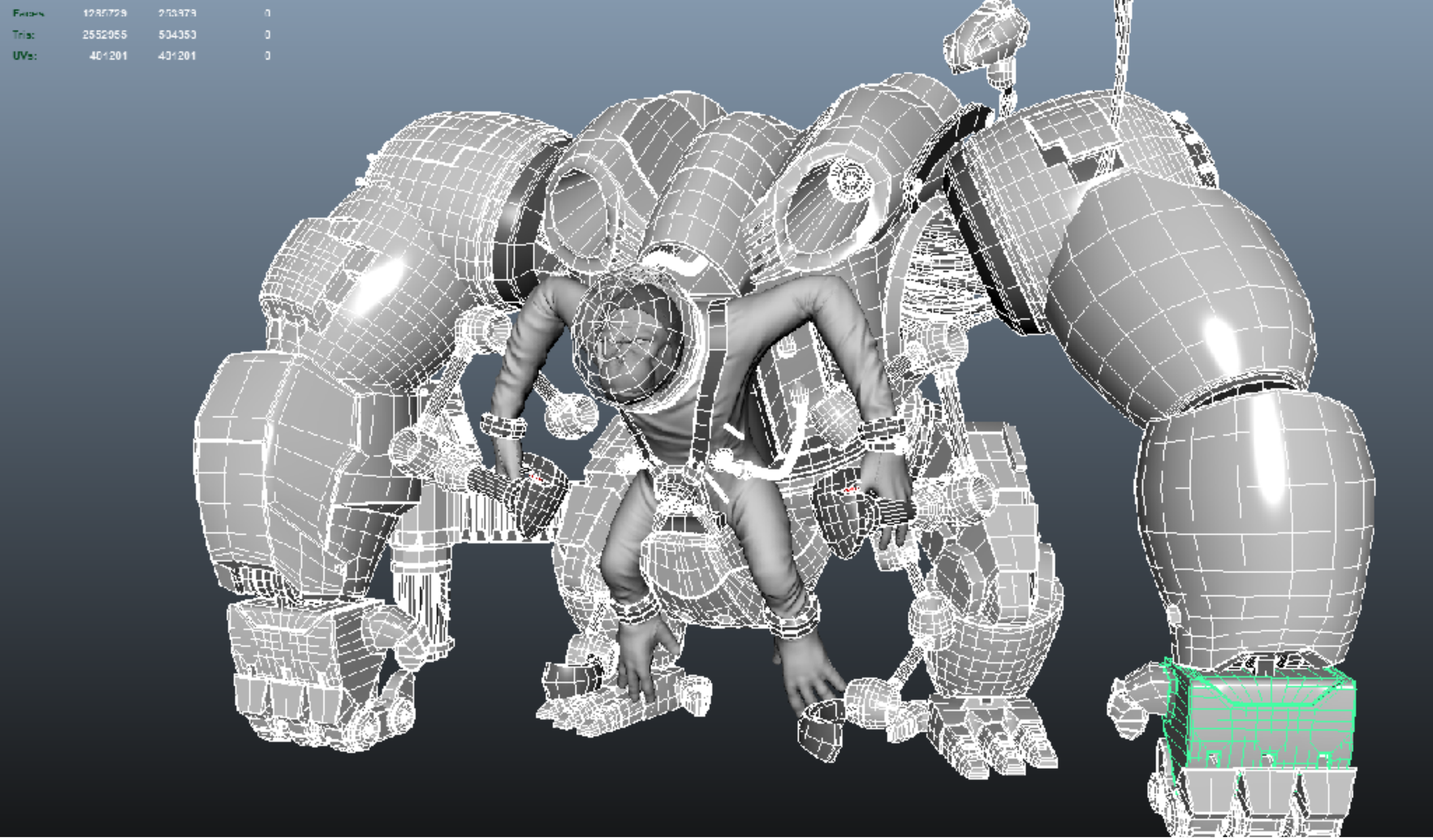
- Let's see now how a GPU works

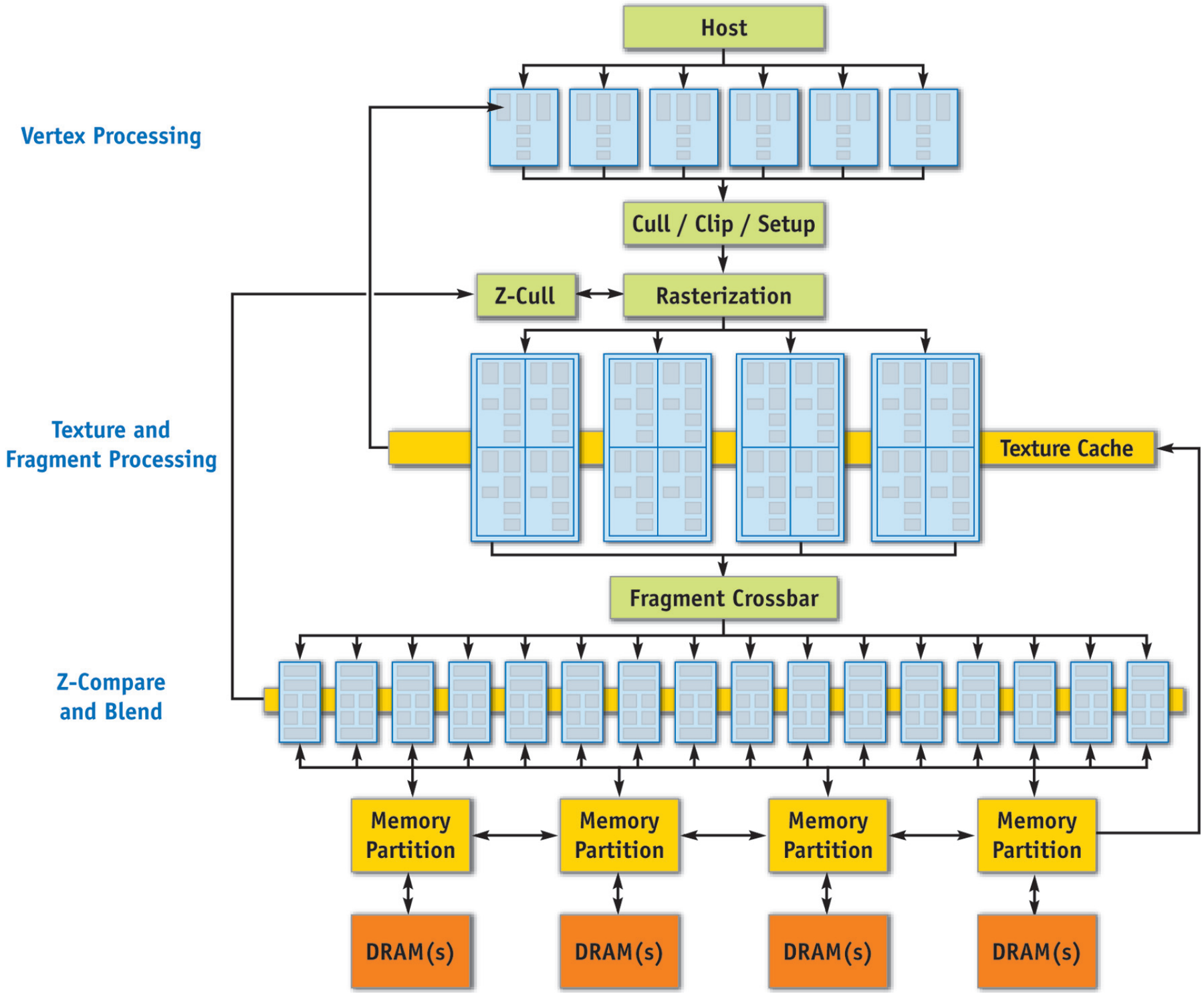
- After, we will see how we can use GPU to achieve way more of just graphics



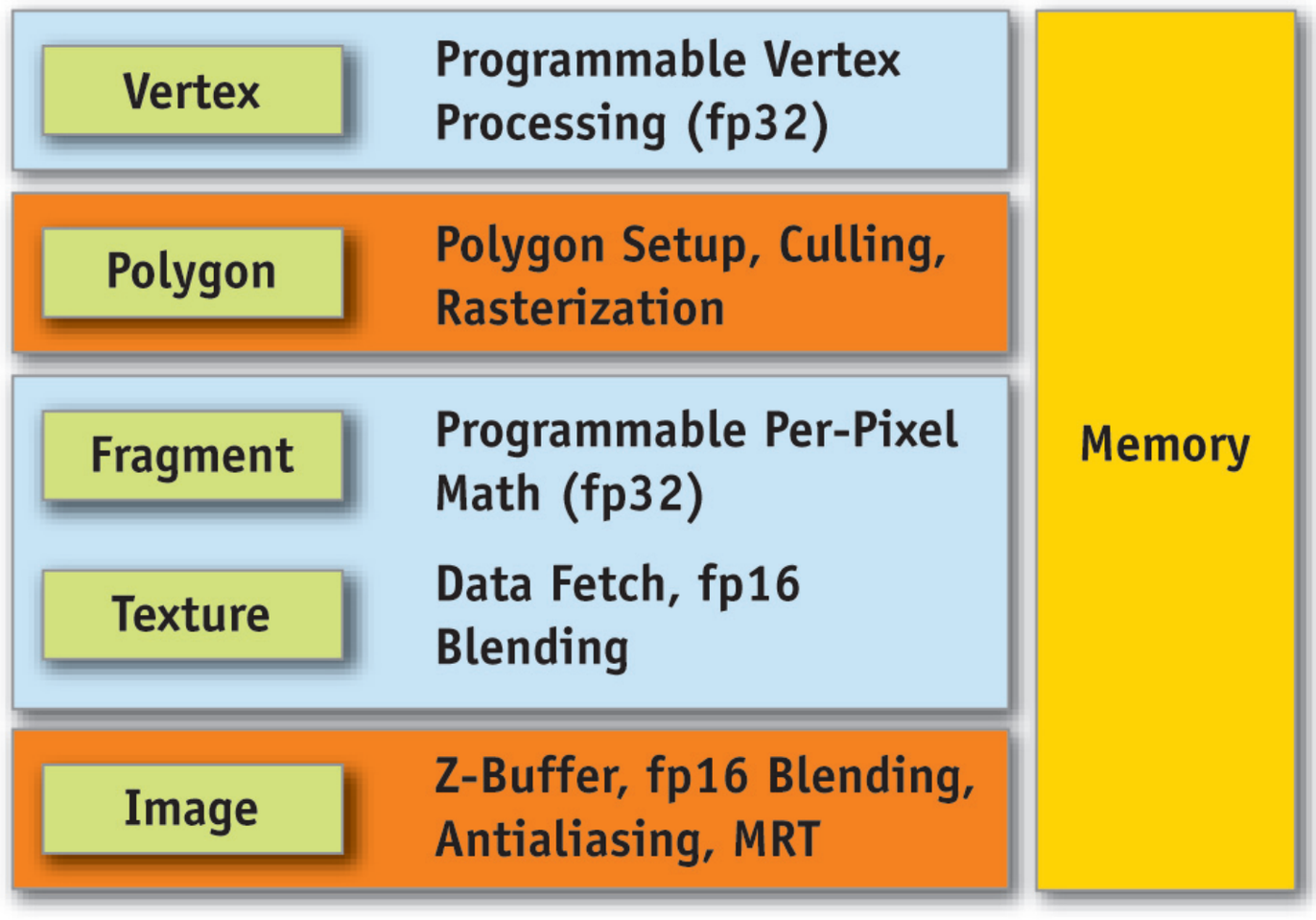
Vertices, Cells, Textures

This mesh will be rendered into pixels

GPU Architecture



Graphics Pipeline



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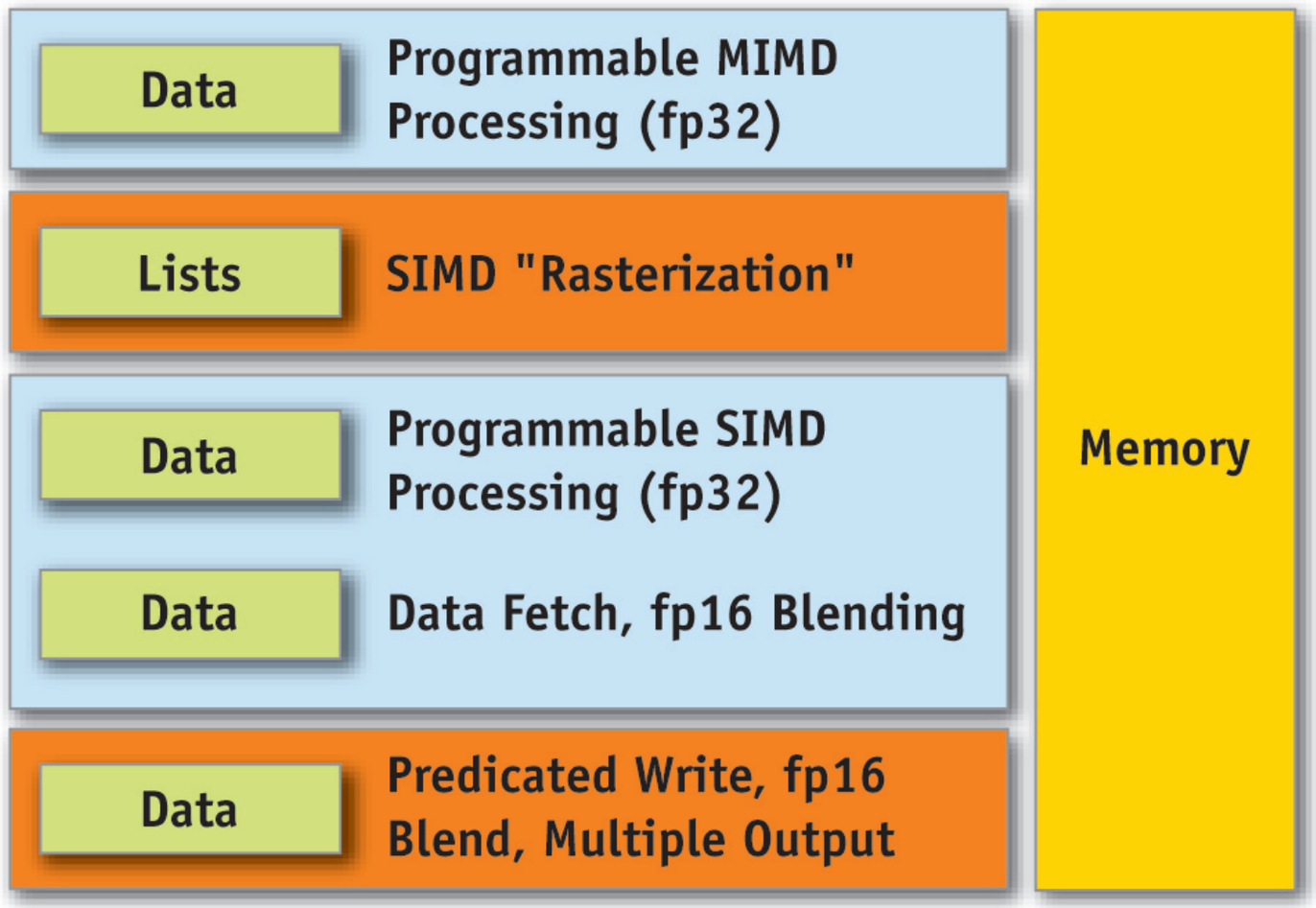
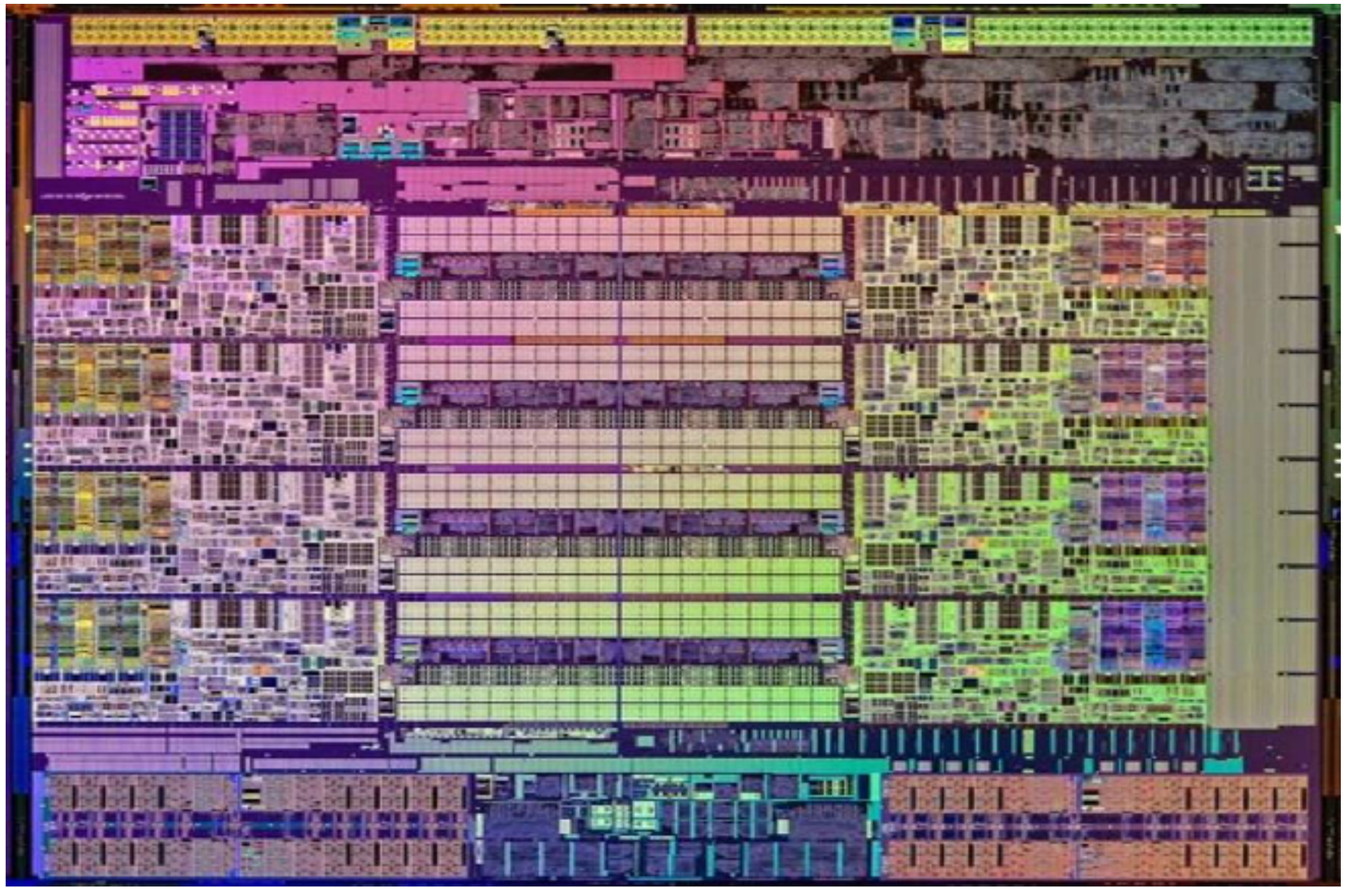


CPU Architecture (Intel i7)



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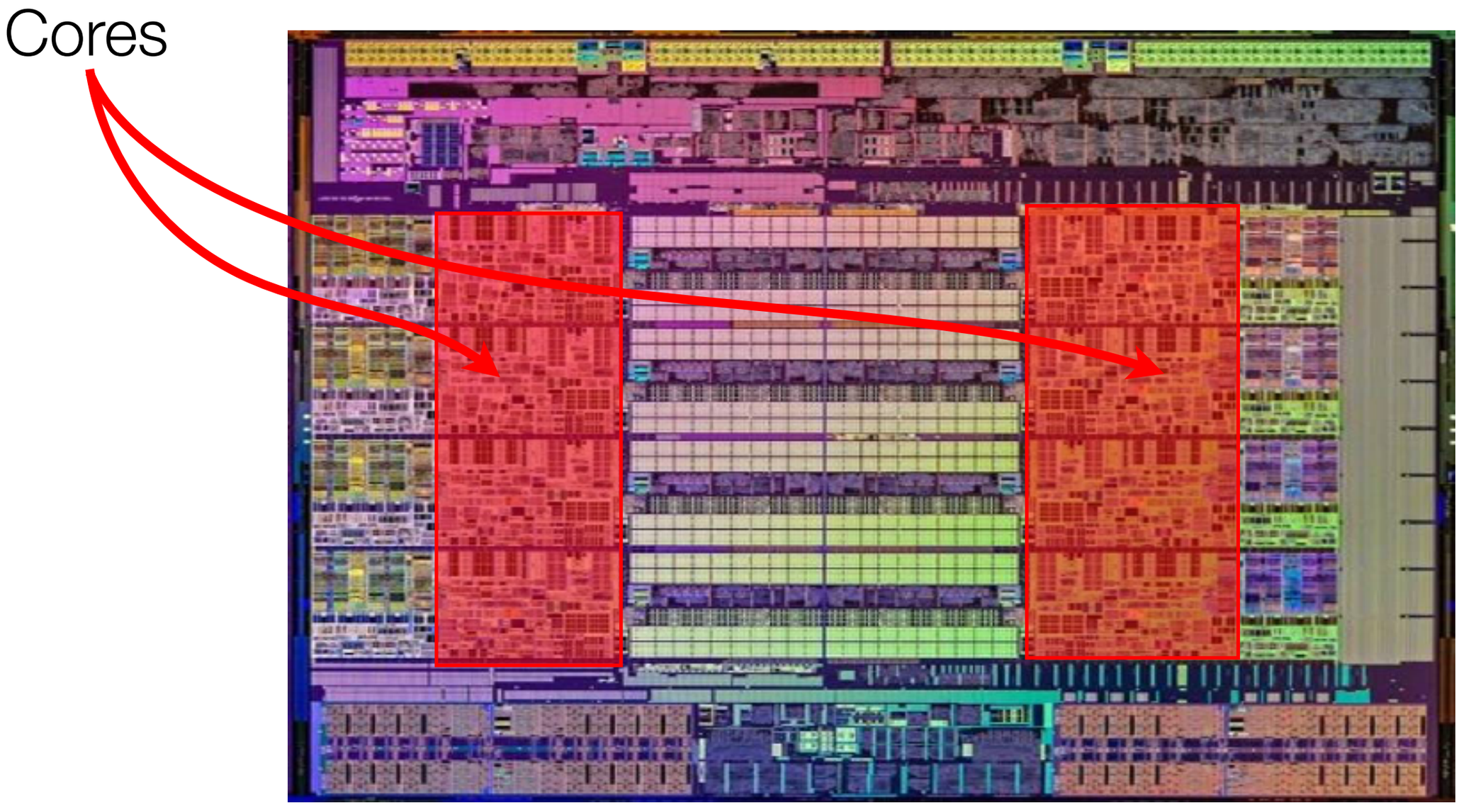

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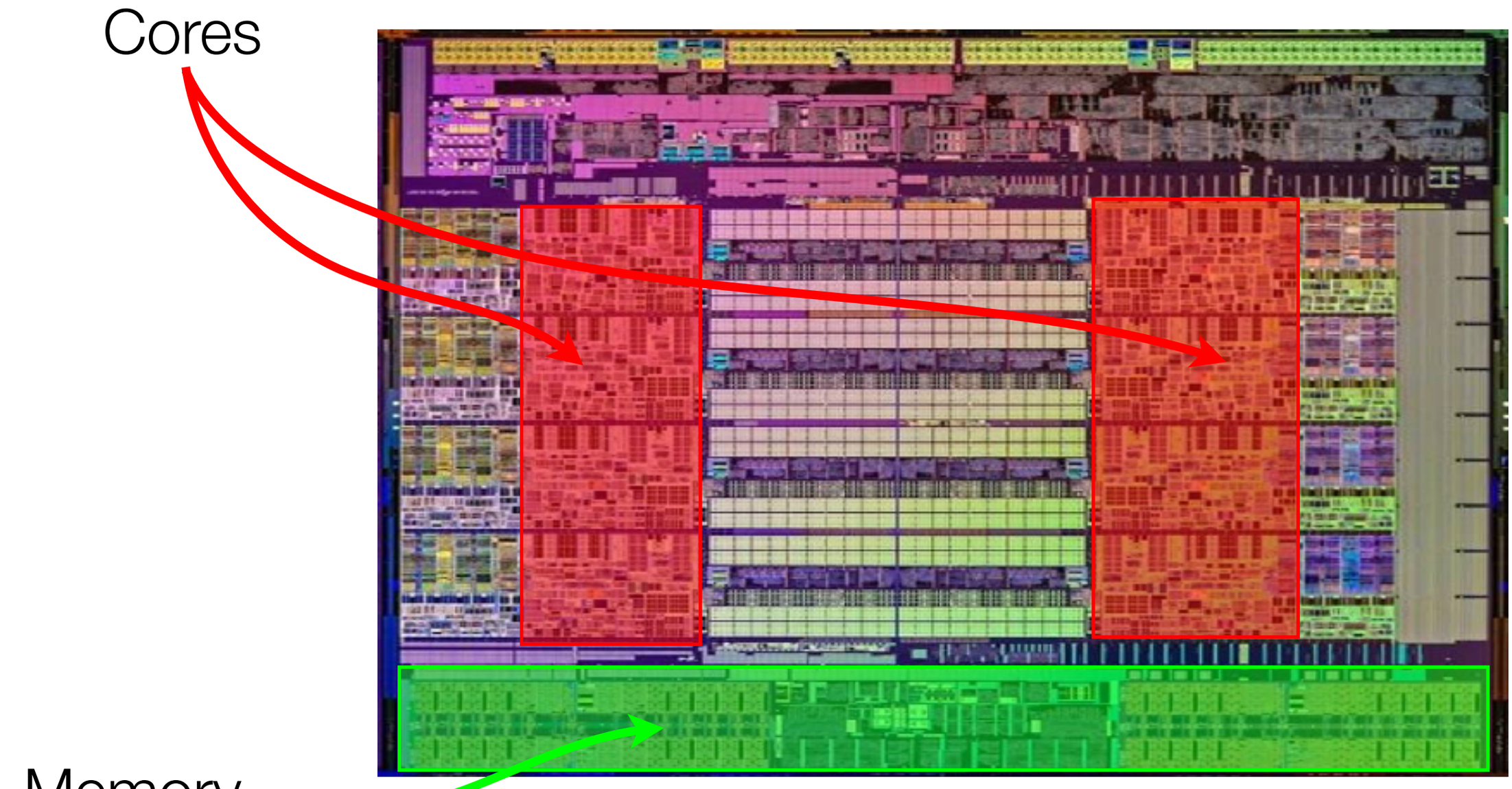

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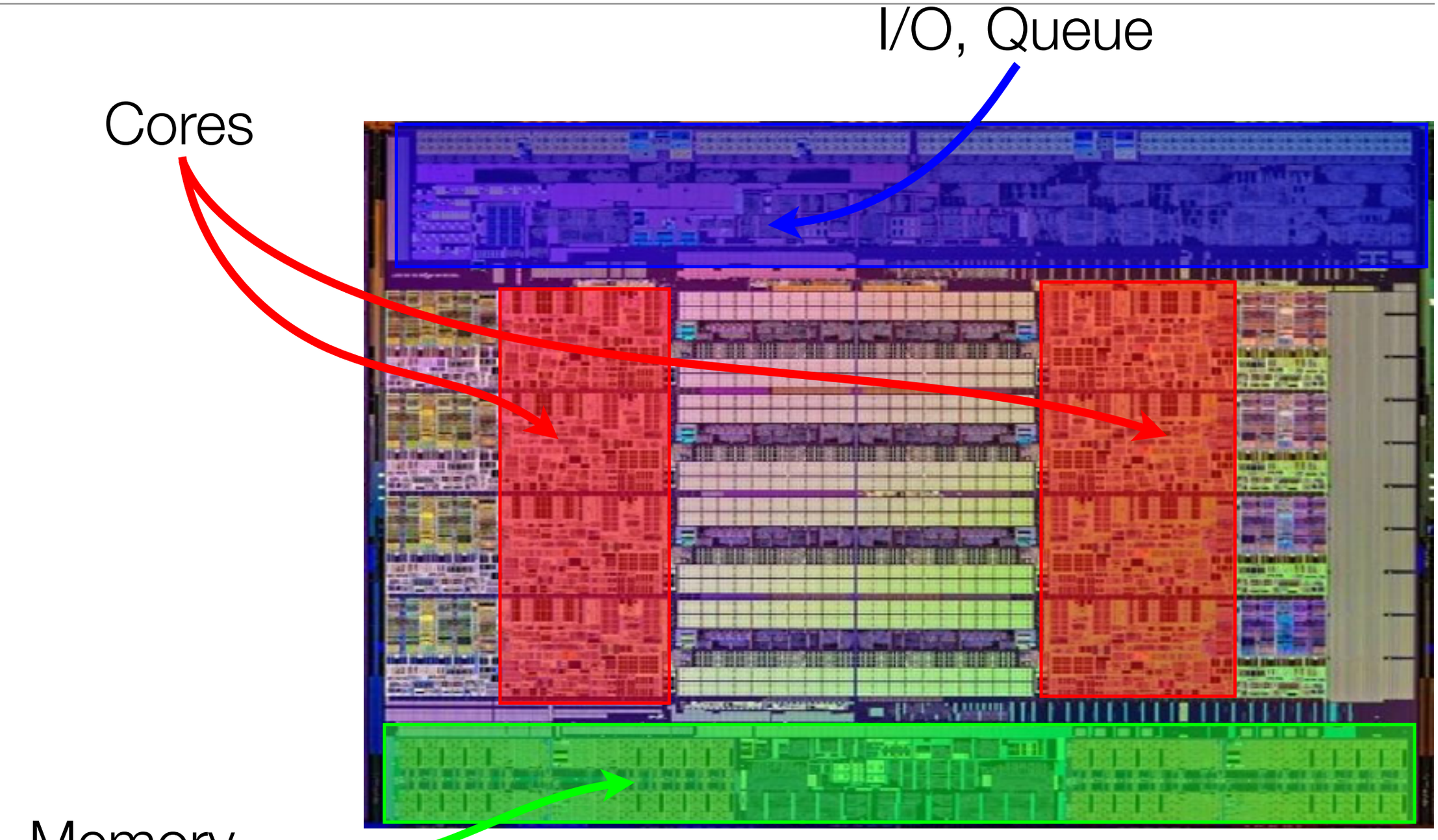

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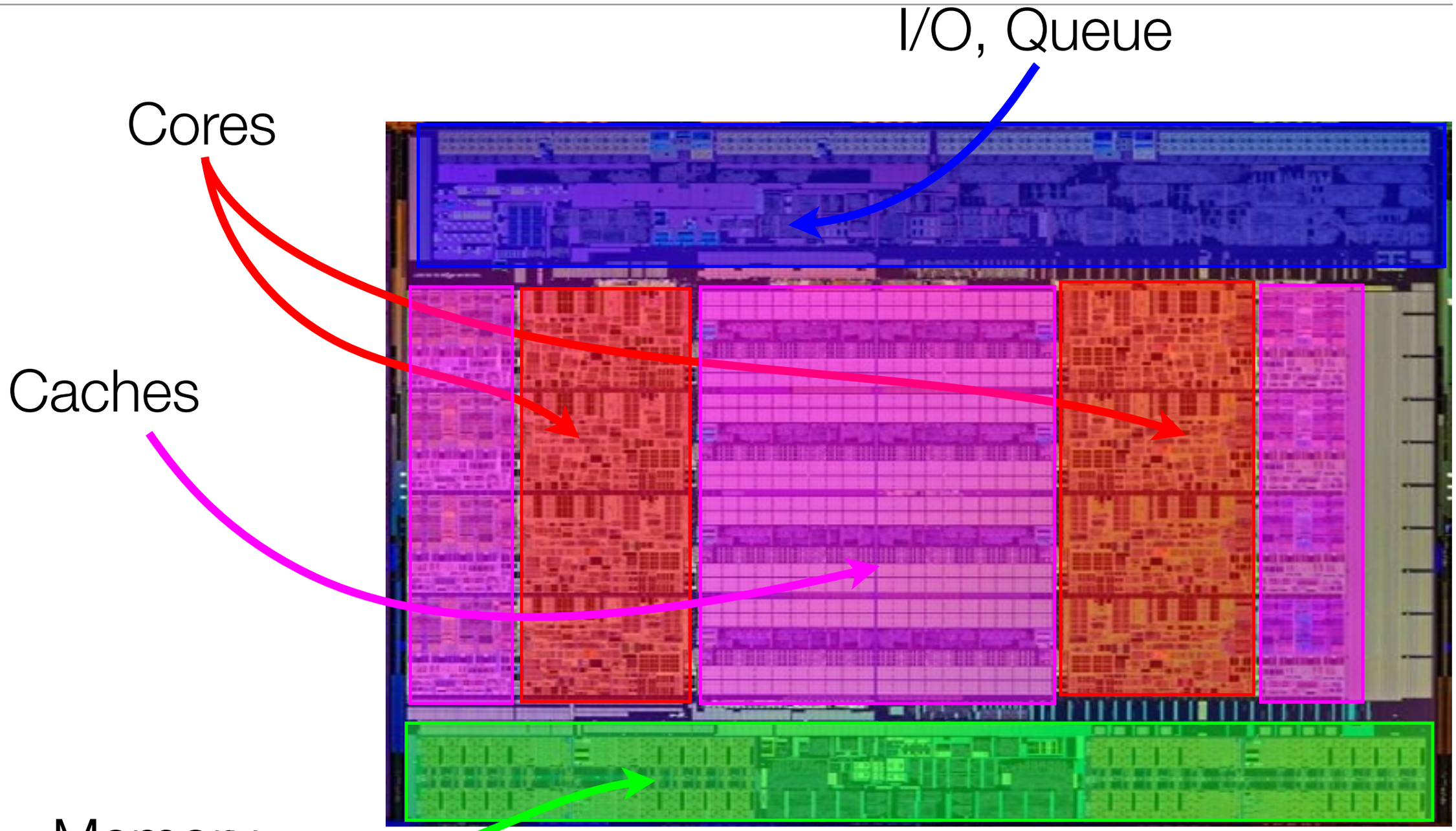

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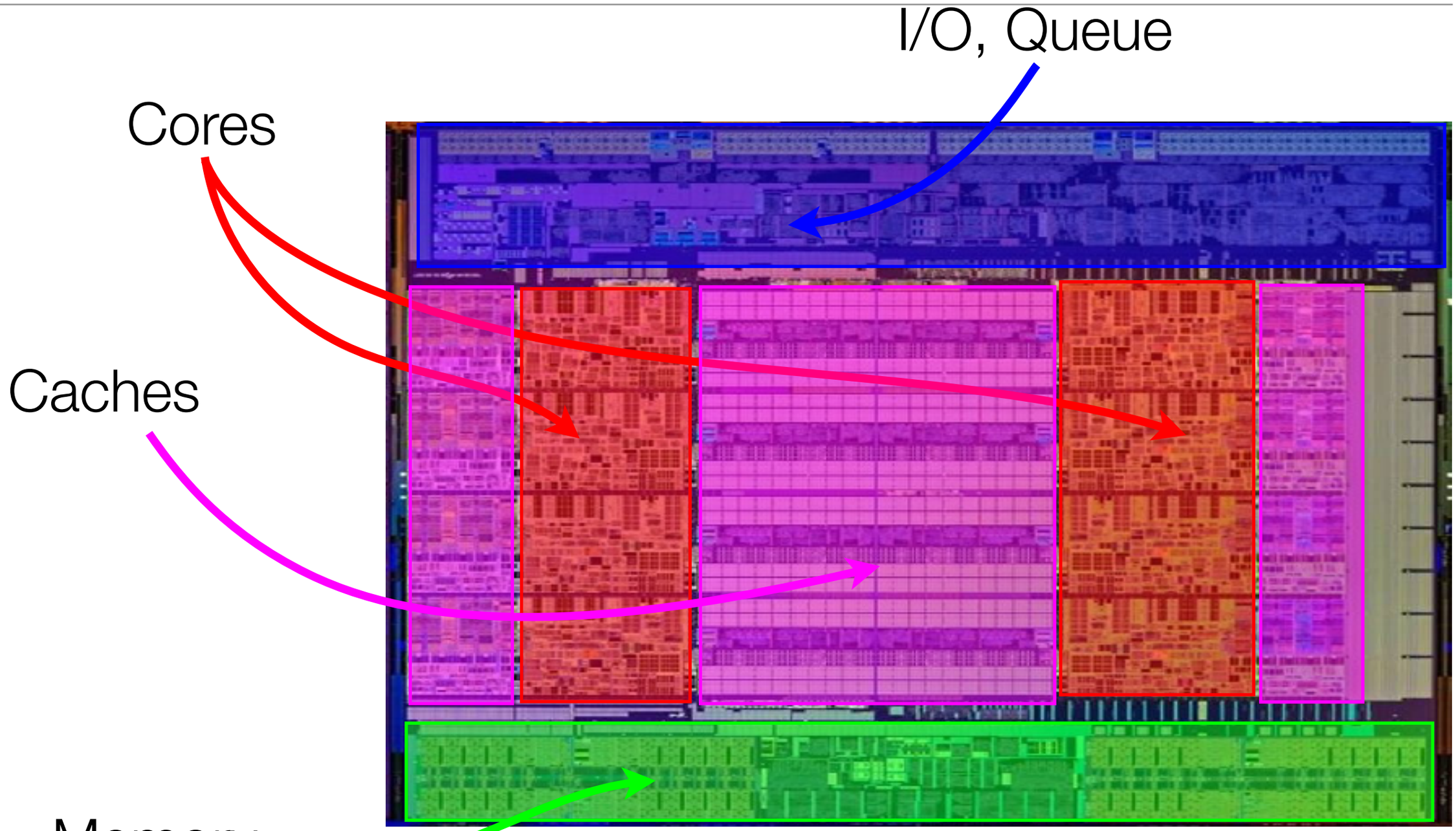

“Multicore” architecture

What if we got rid of everything?

CPU Architecture

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Chip

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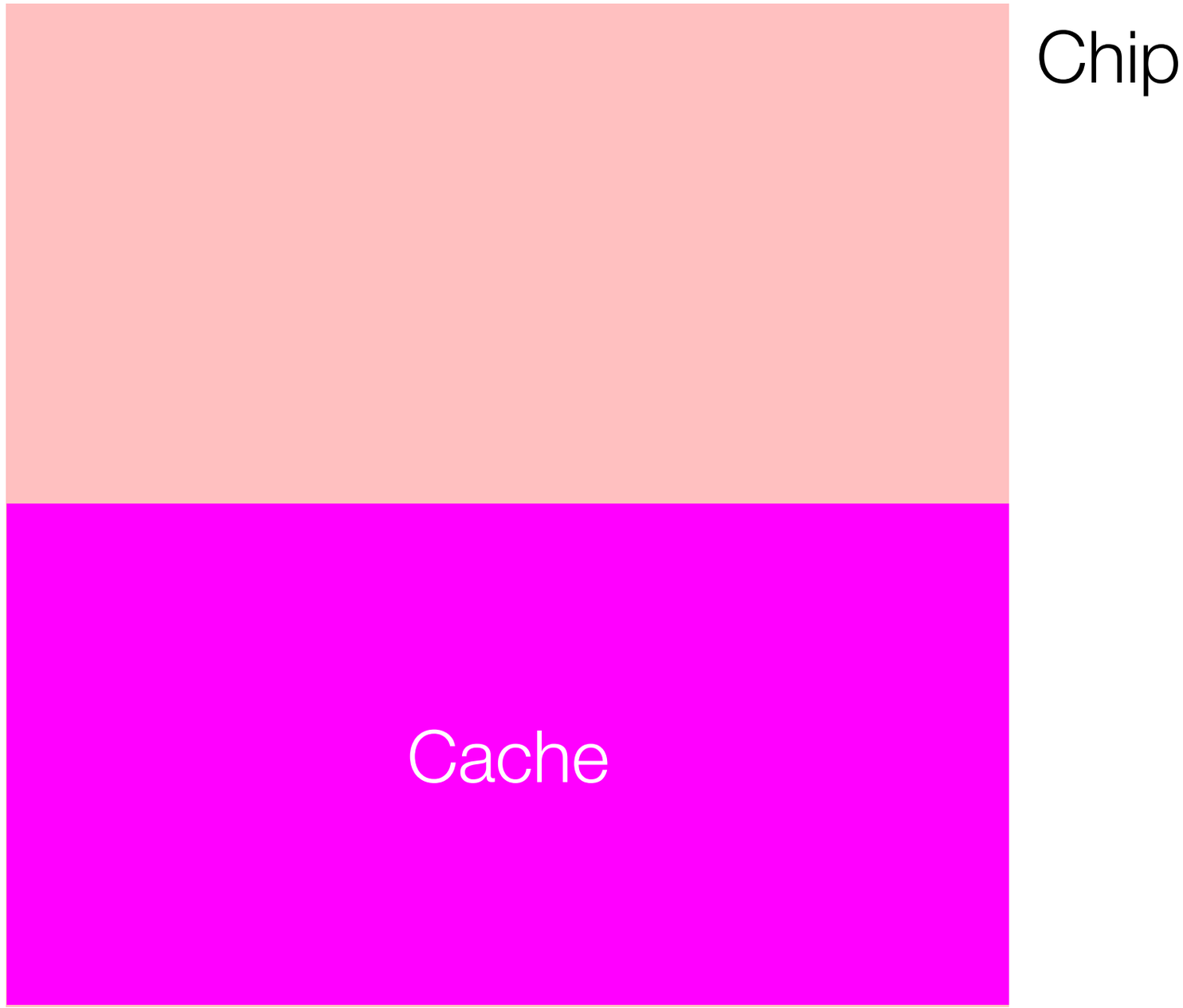

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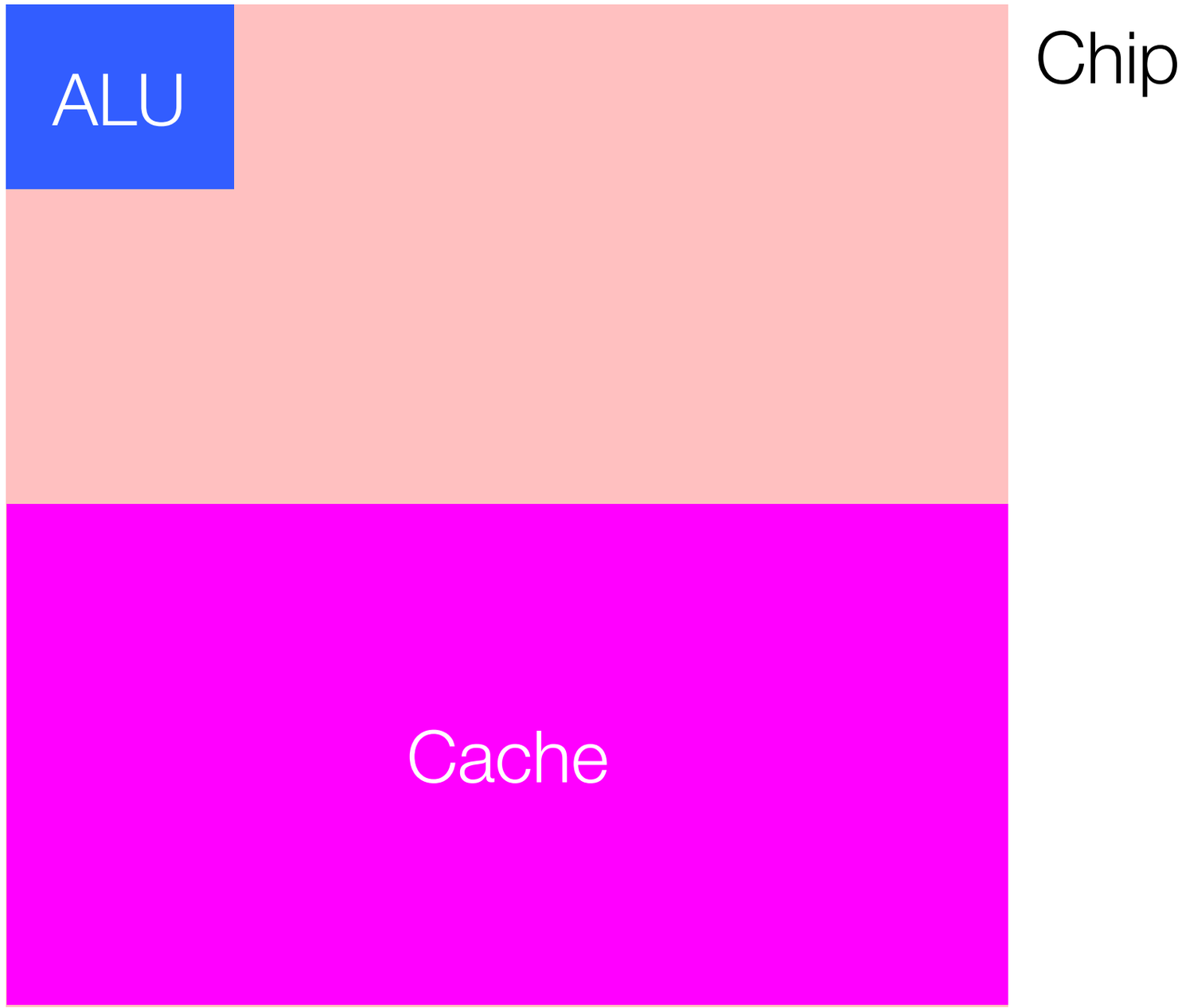

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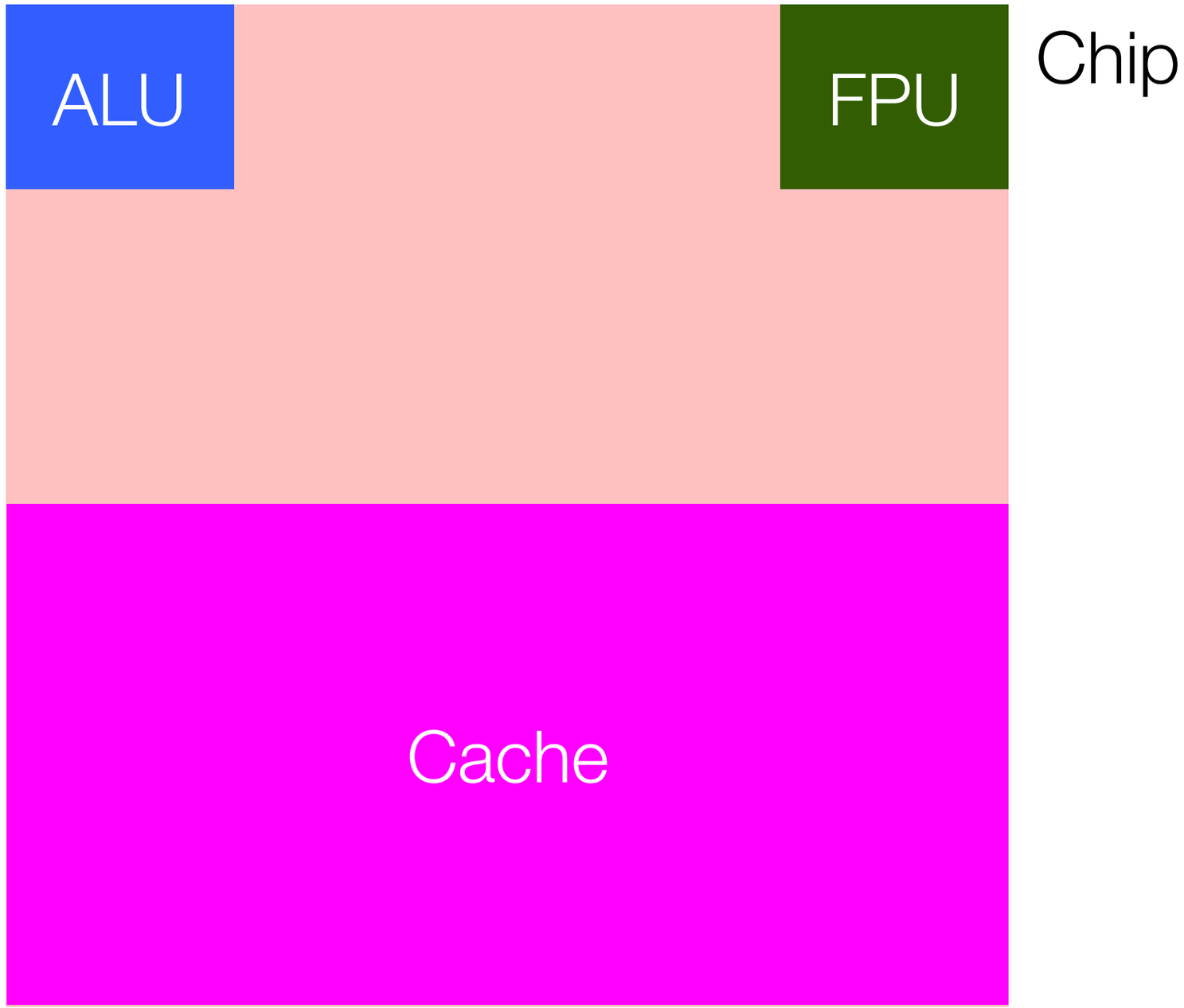

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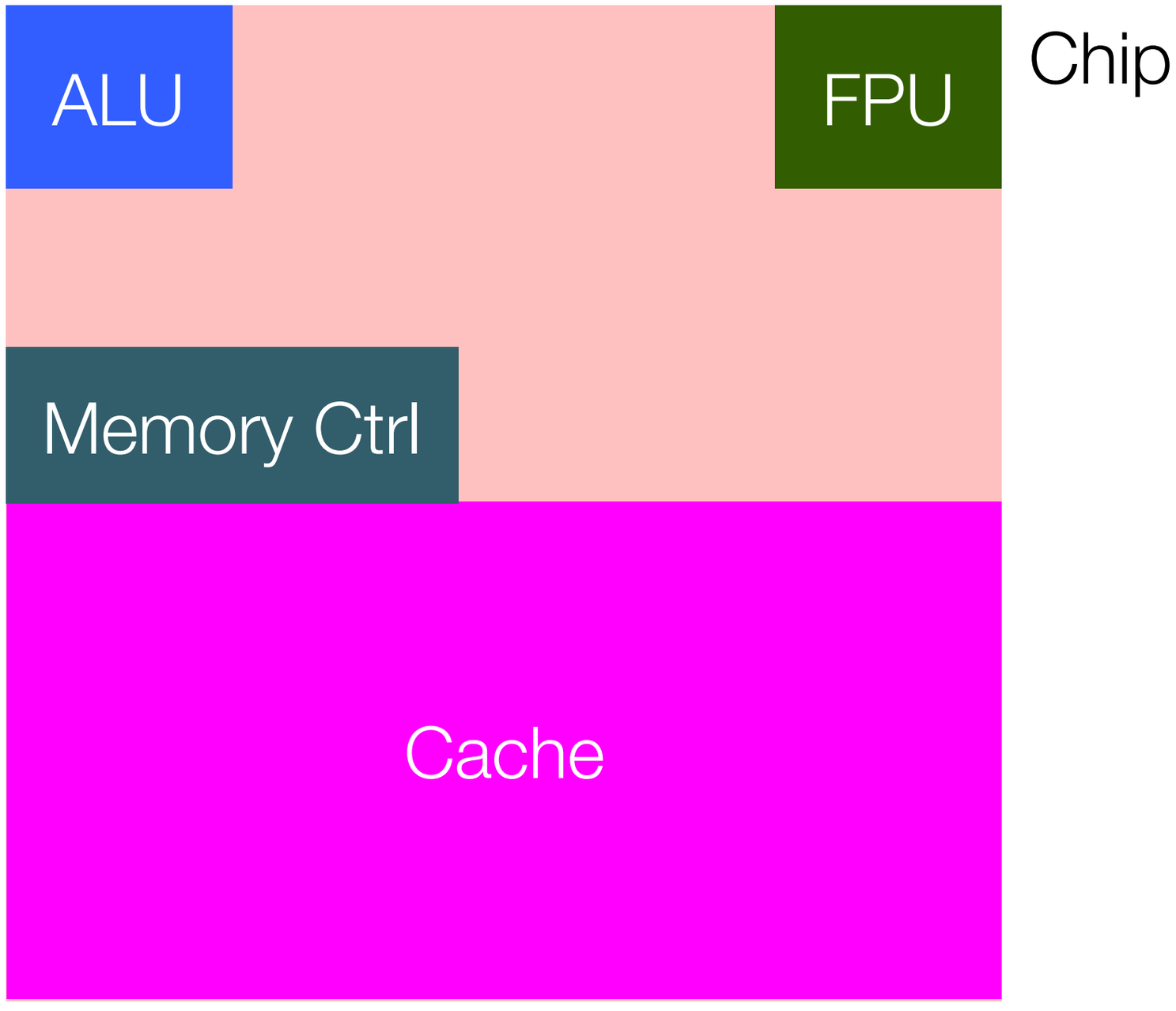

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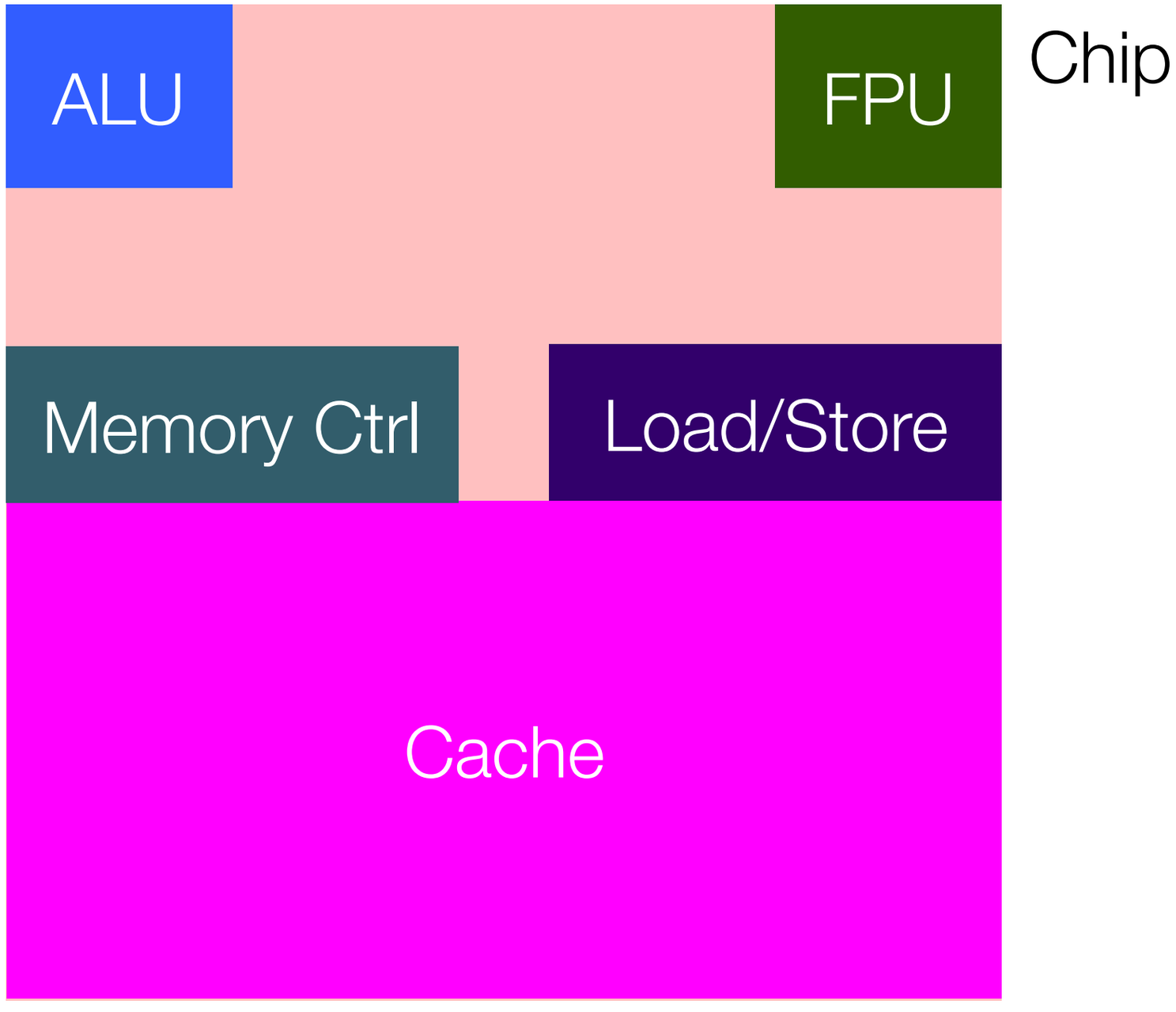

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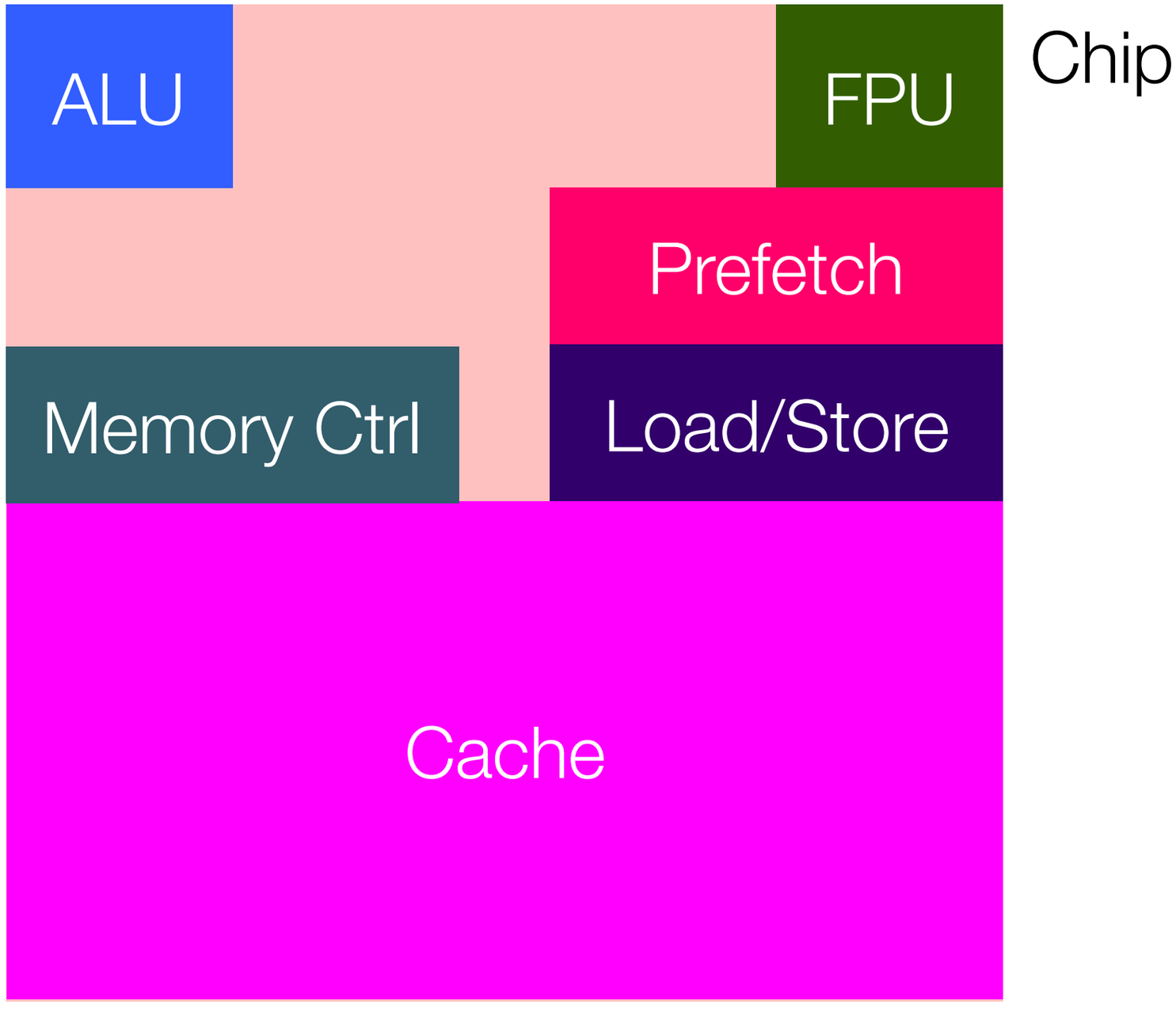

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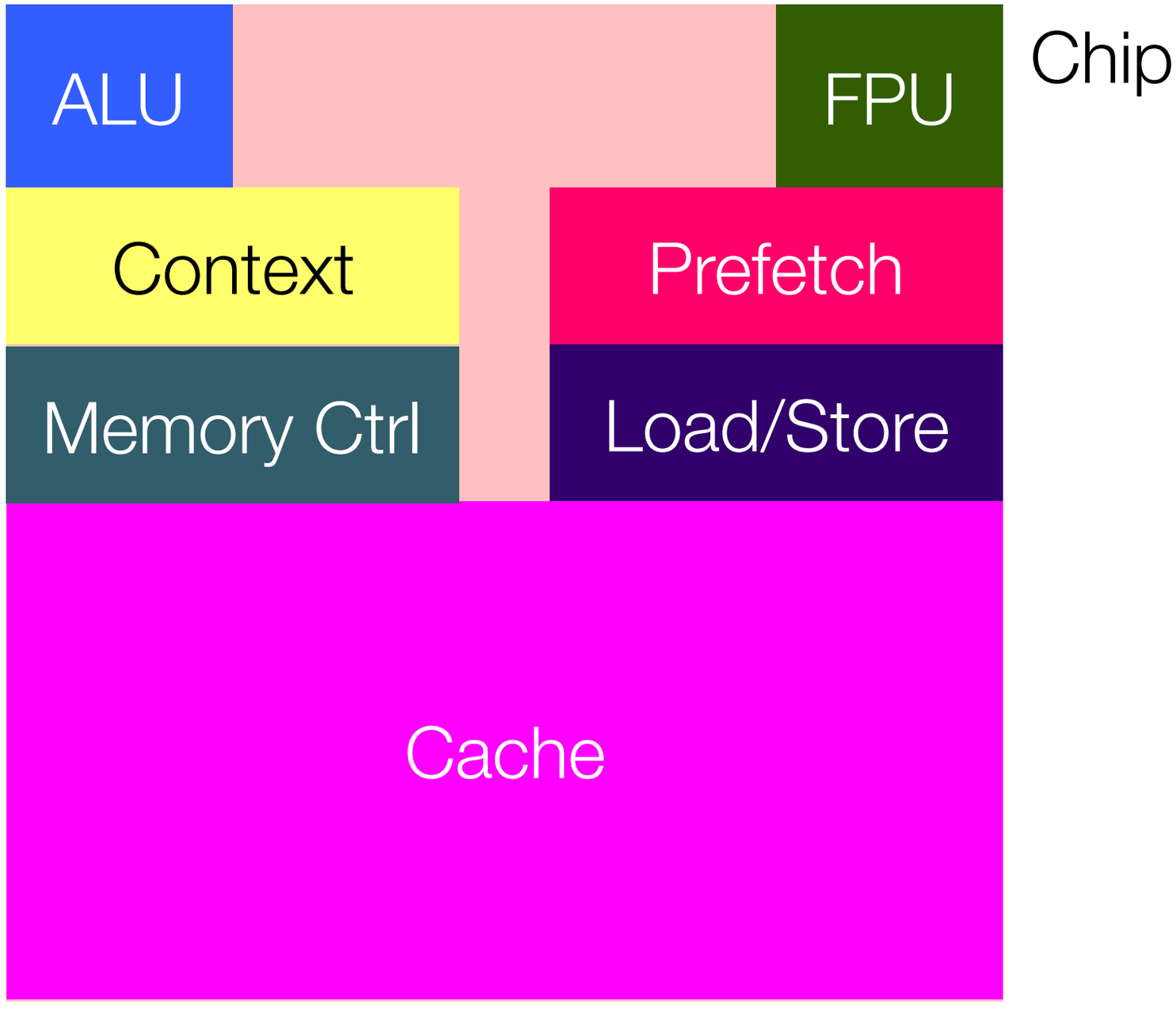

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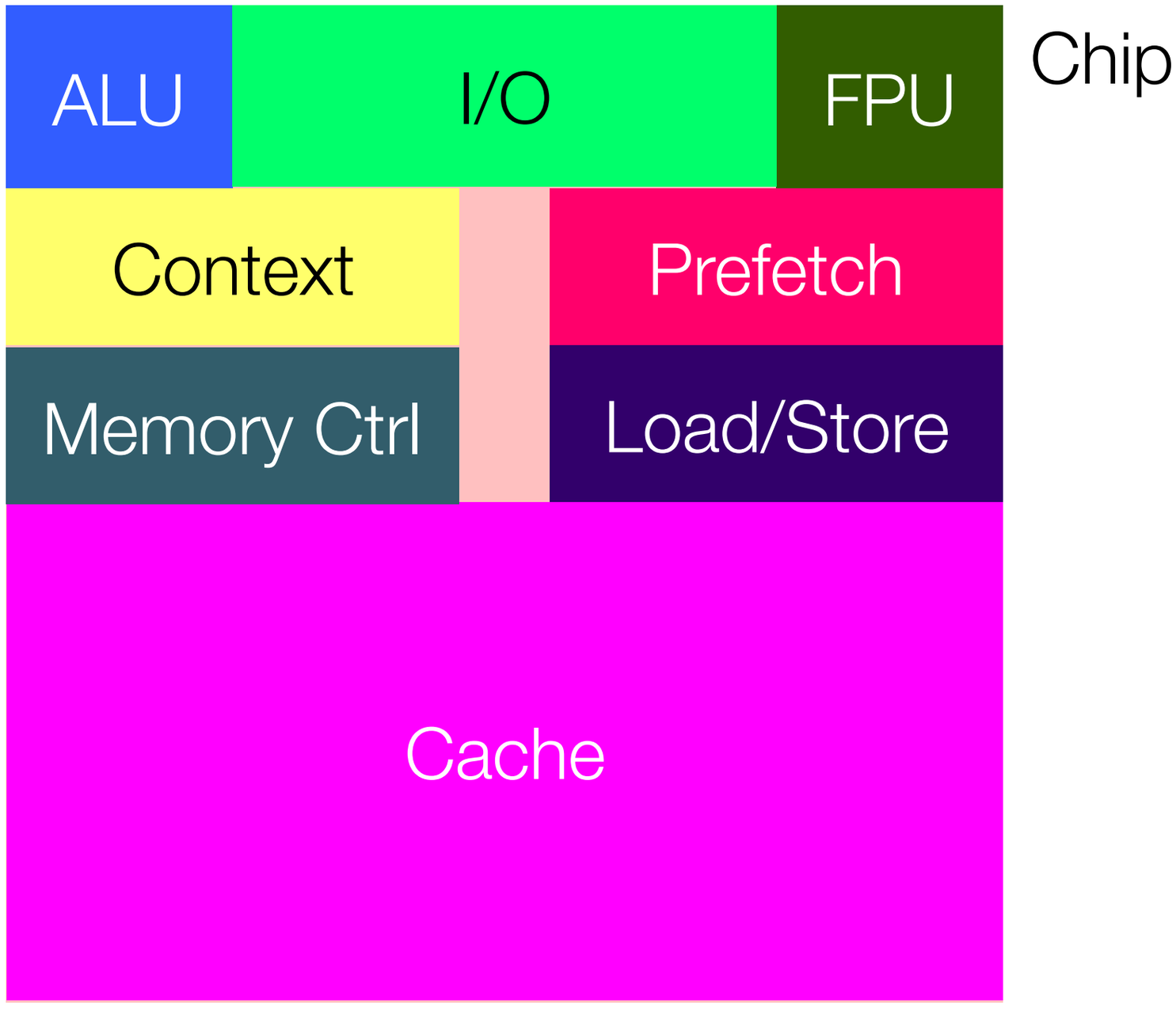

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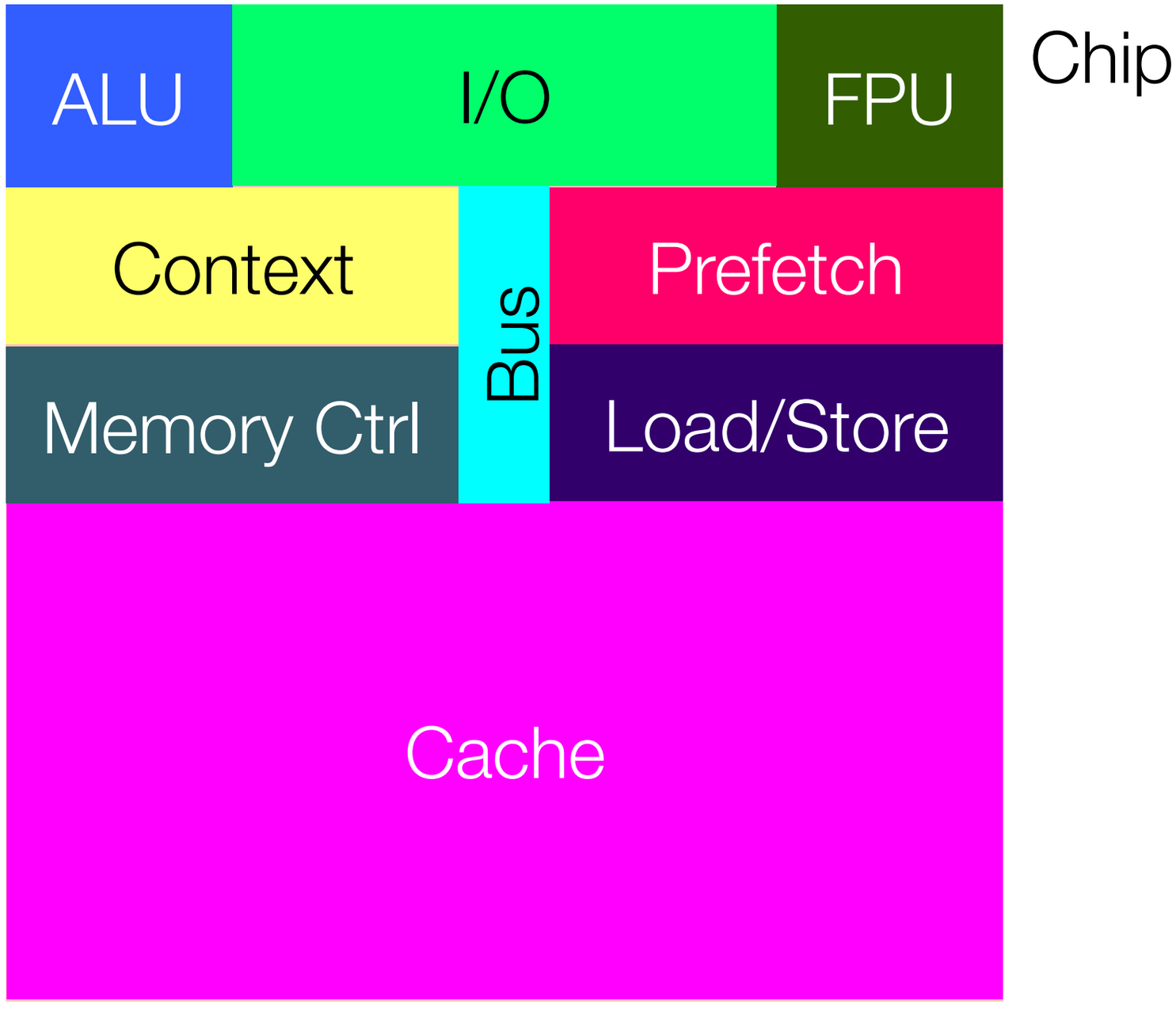

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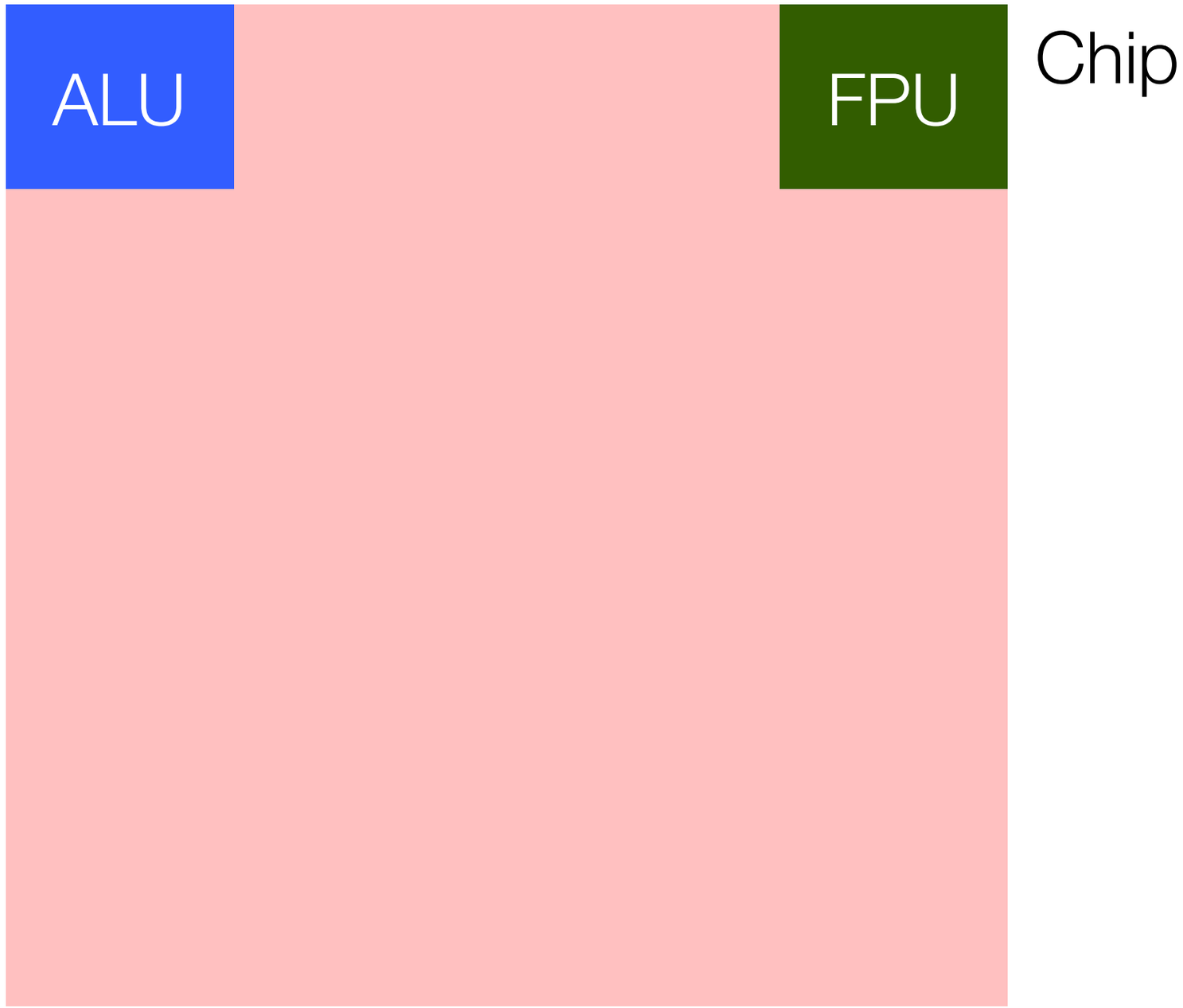

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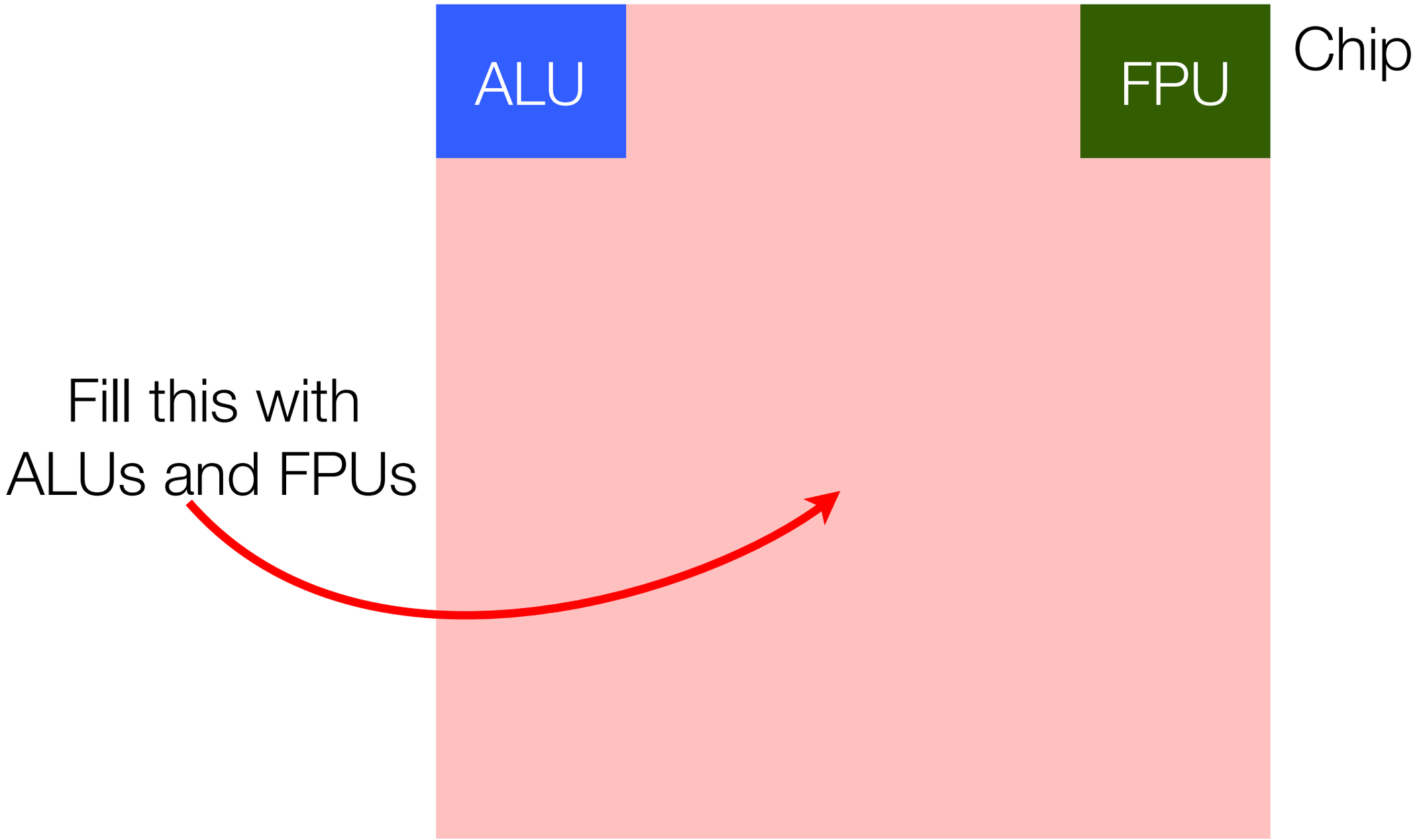

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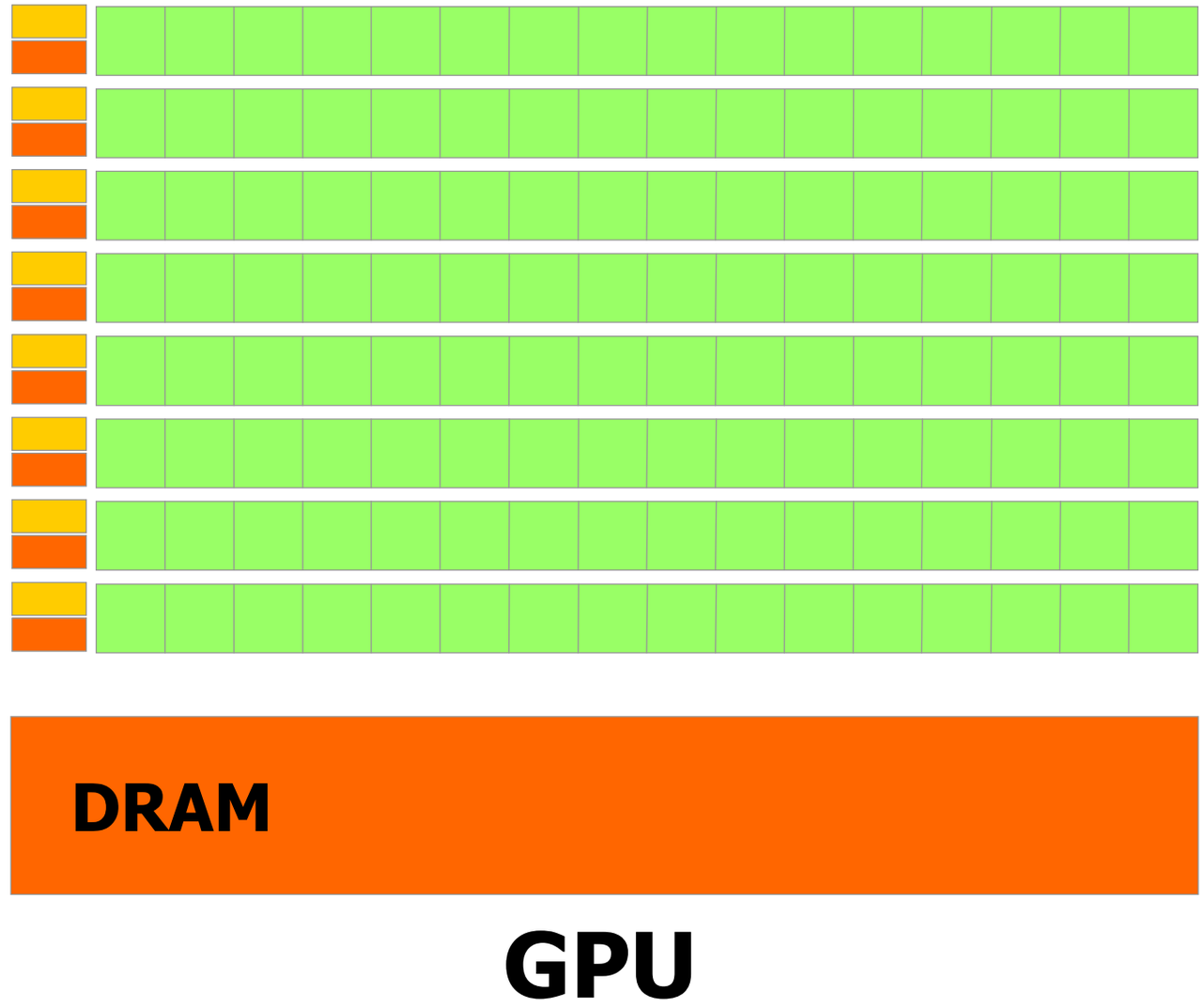
- Since GPUs actually *share control* among cores, one single instruction is executed by several threads at once by adding execution units instead of control ones

SIMD Architecture



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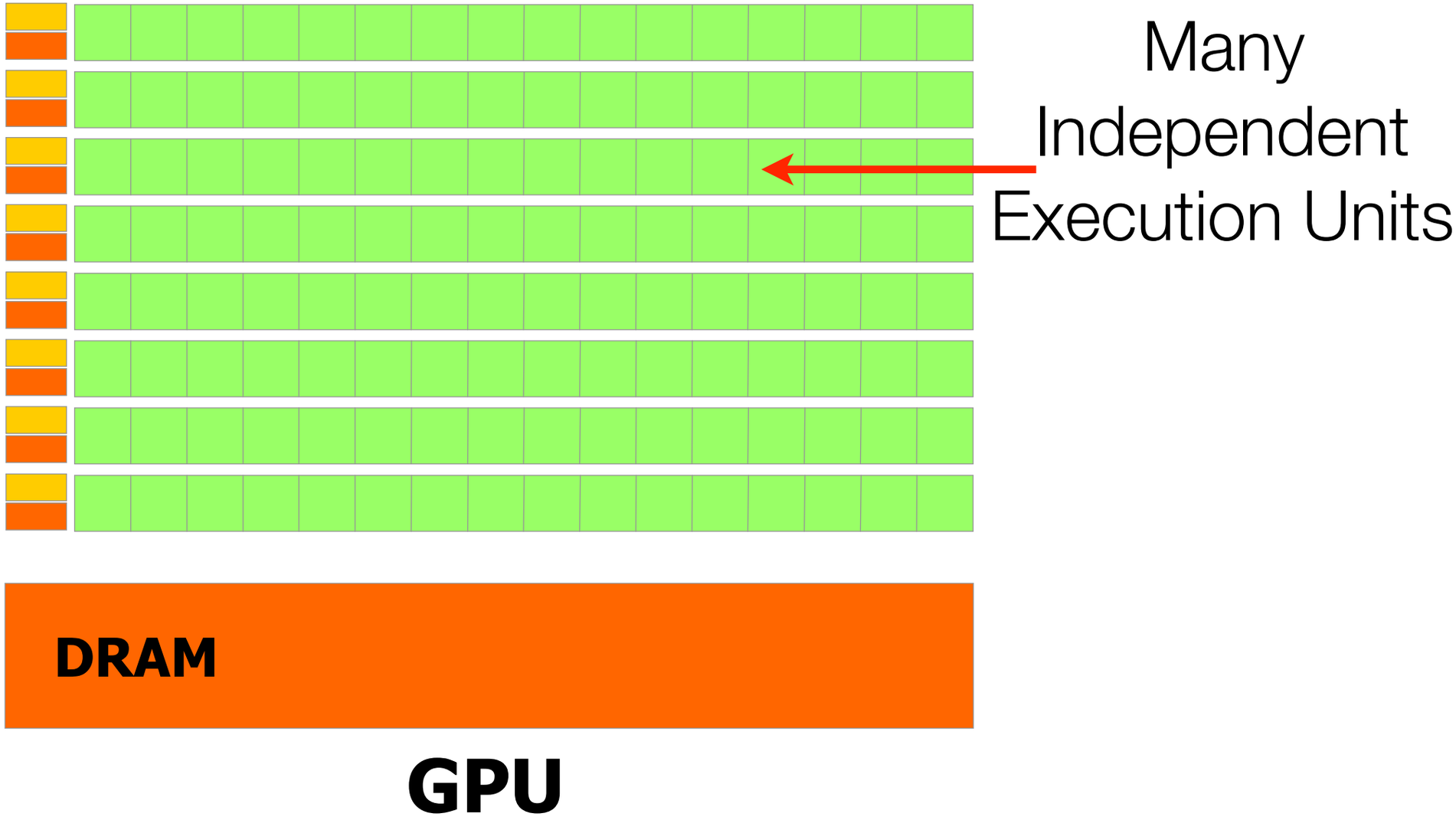

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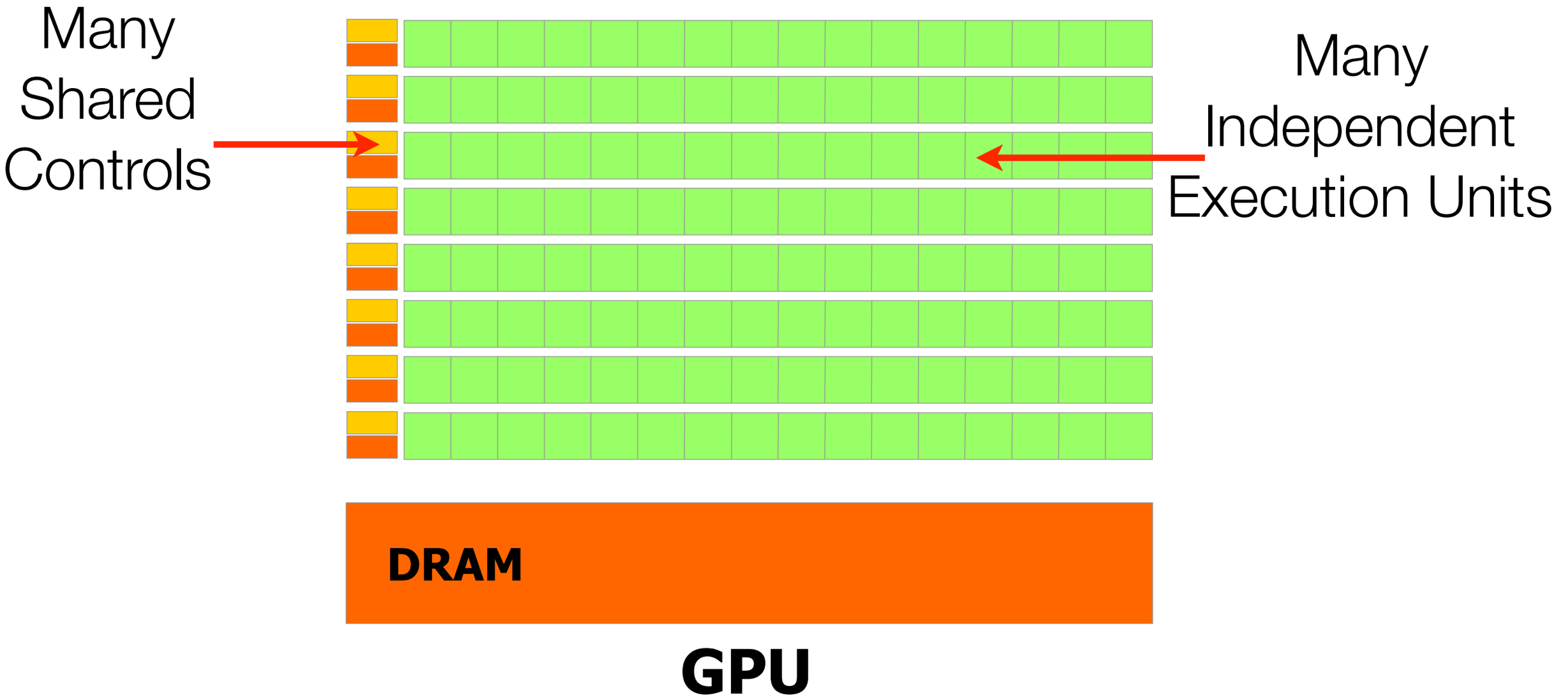

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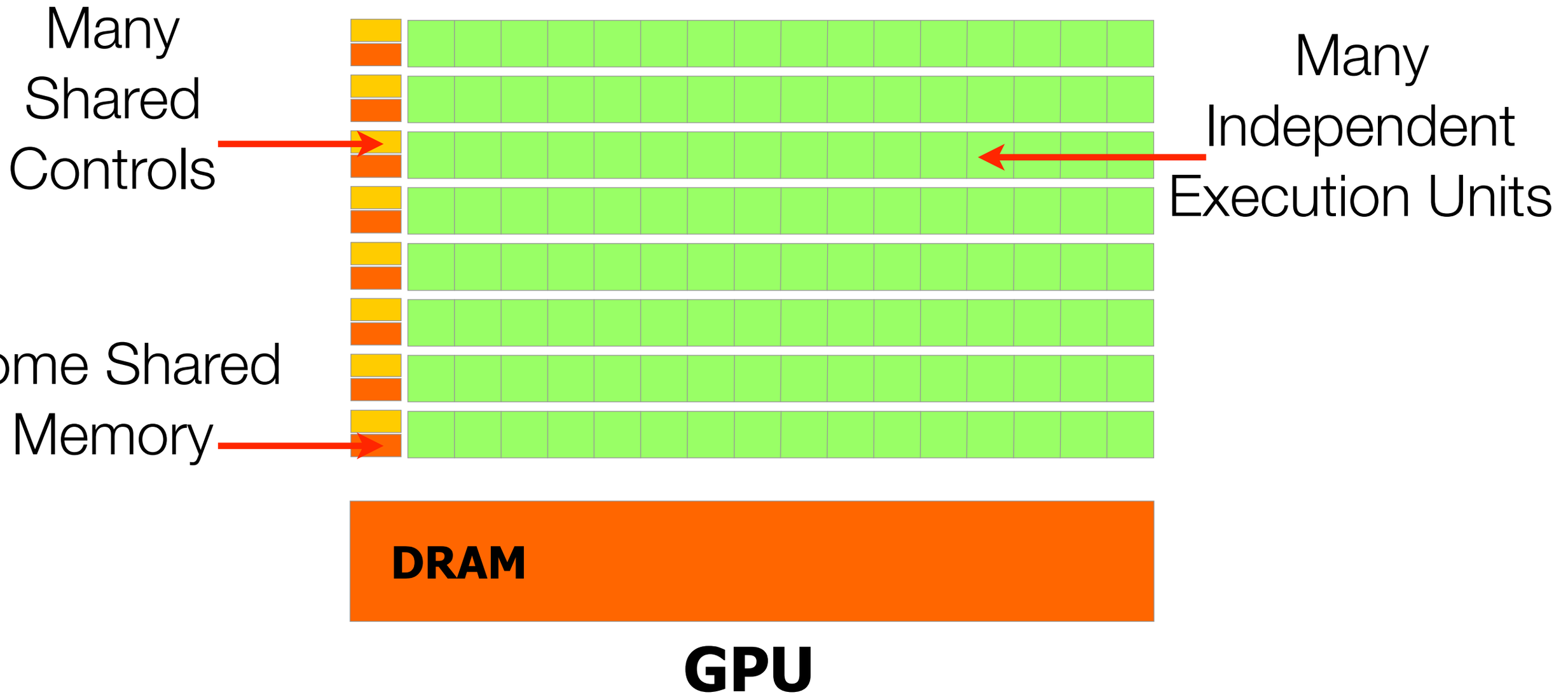

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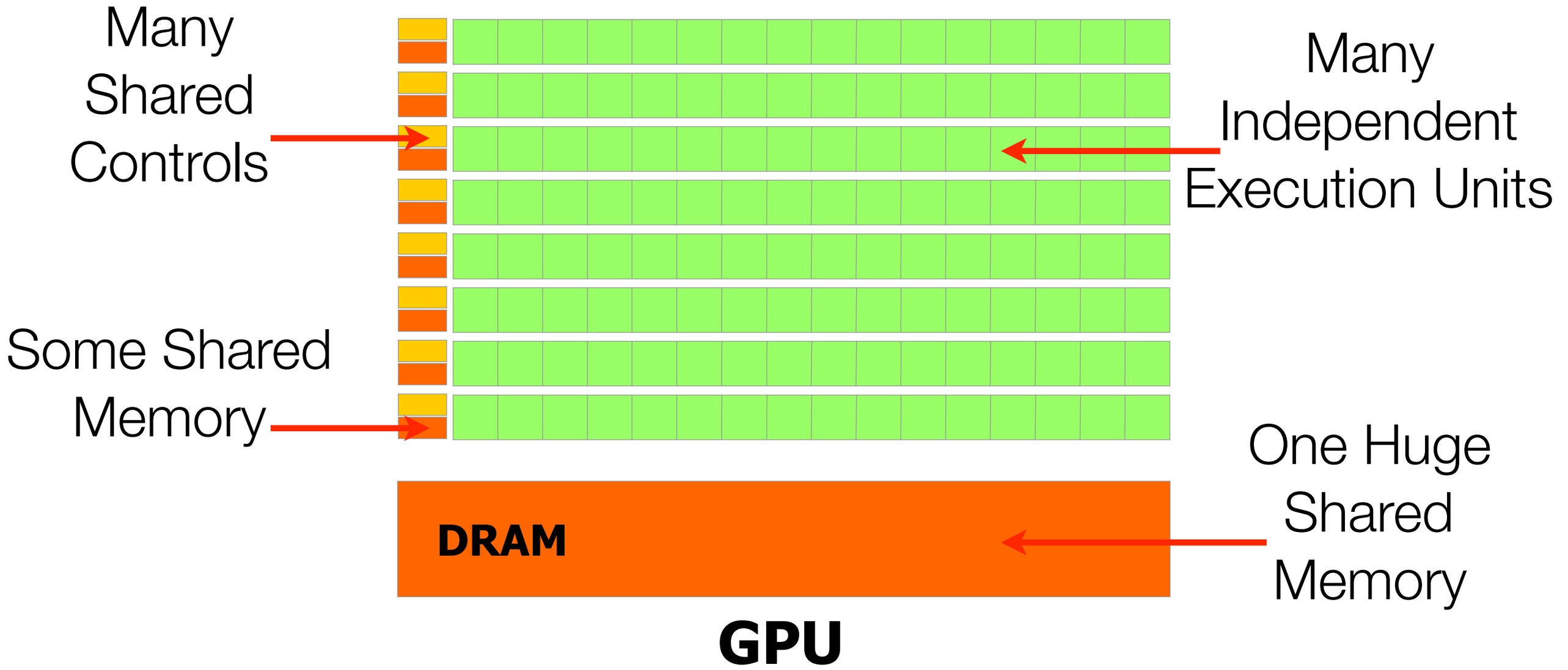

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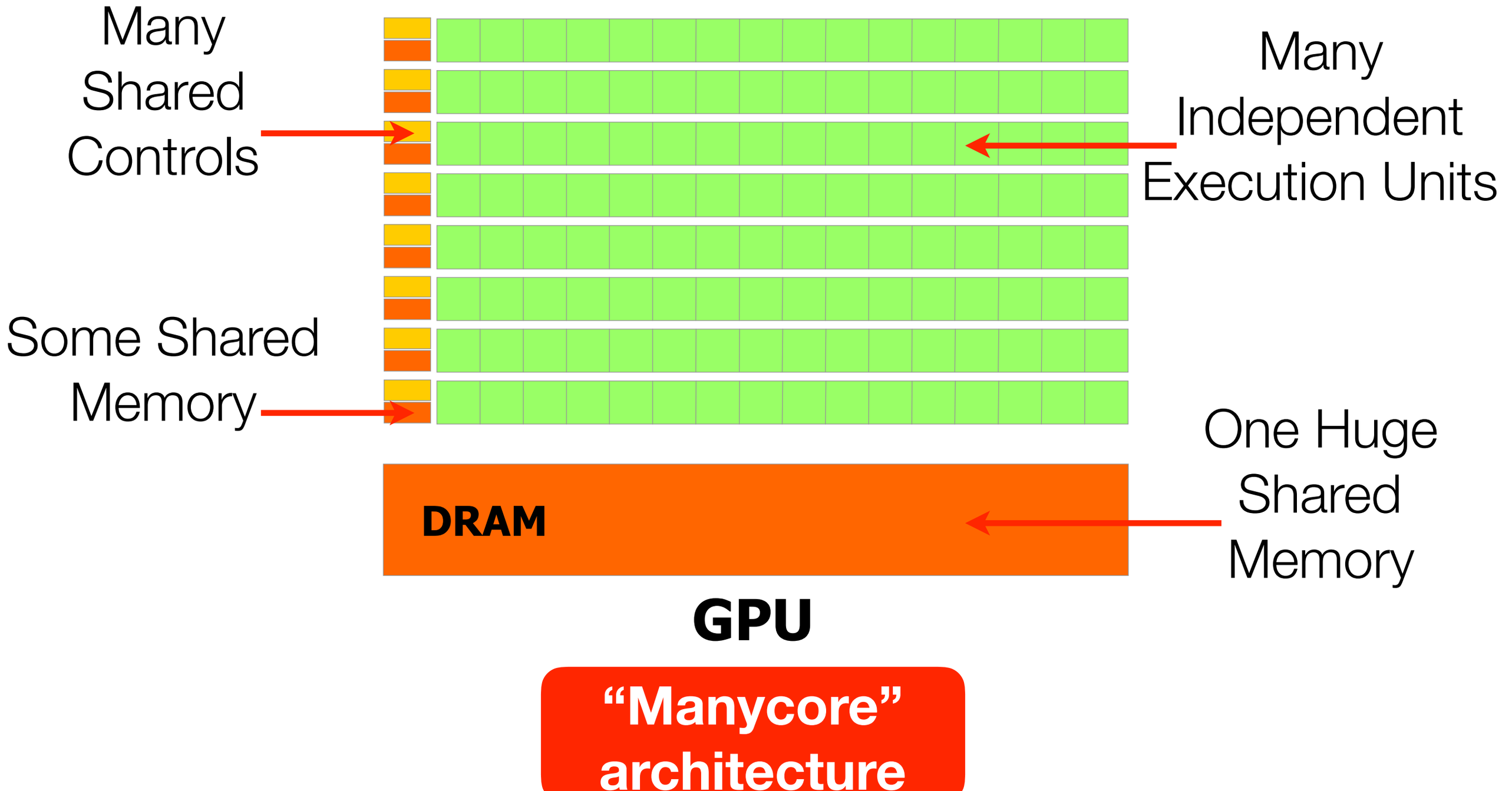

“Manycore” architecture

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- It runs the same program on different GPUs

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{
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}

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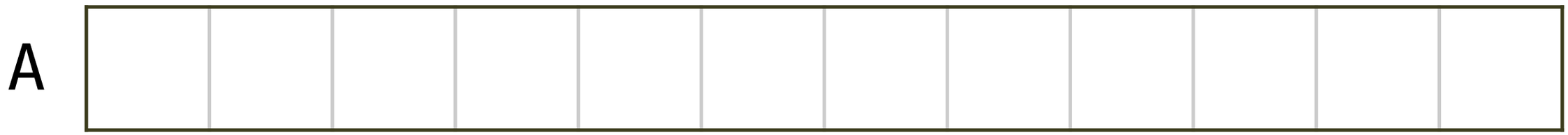

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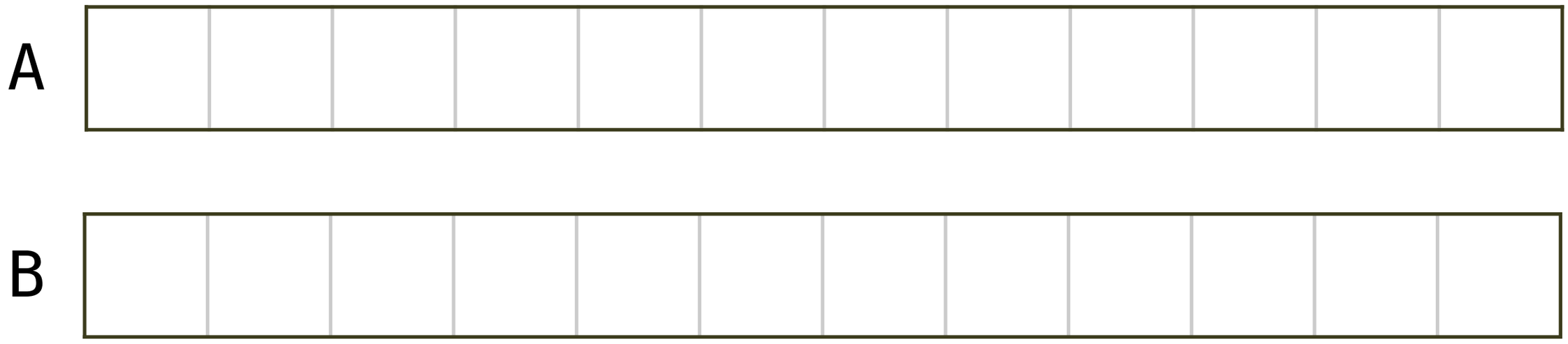

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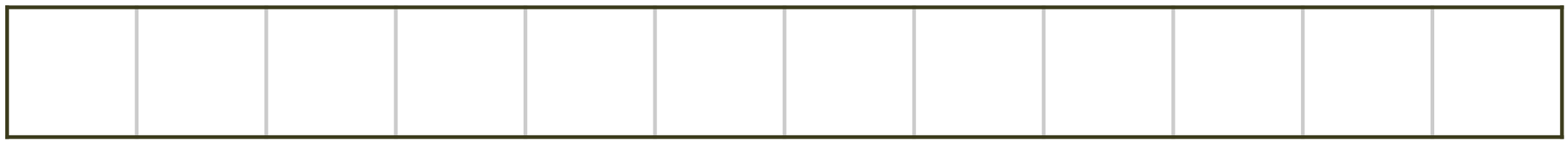

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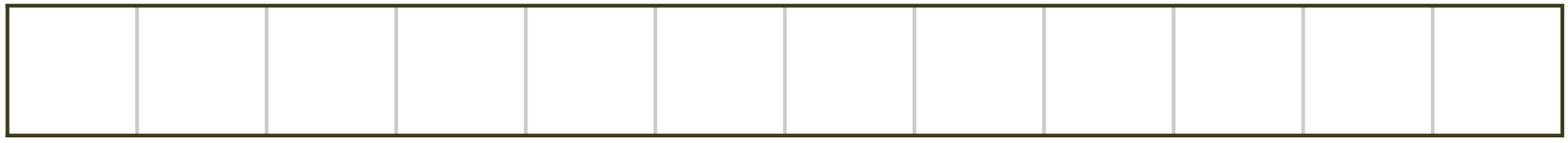

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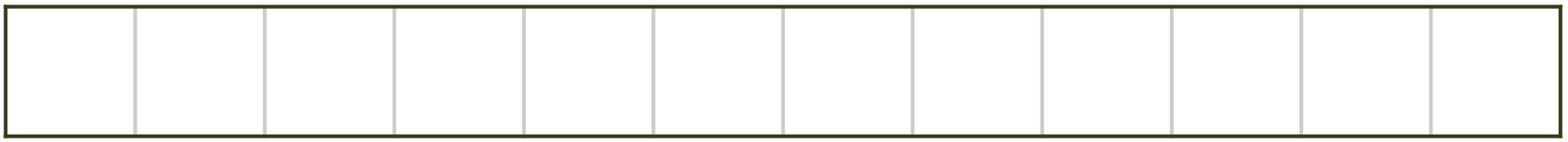

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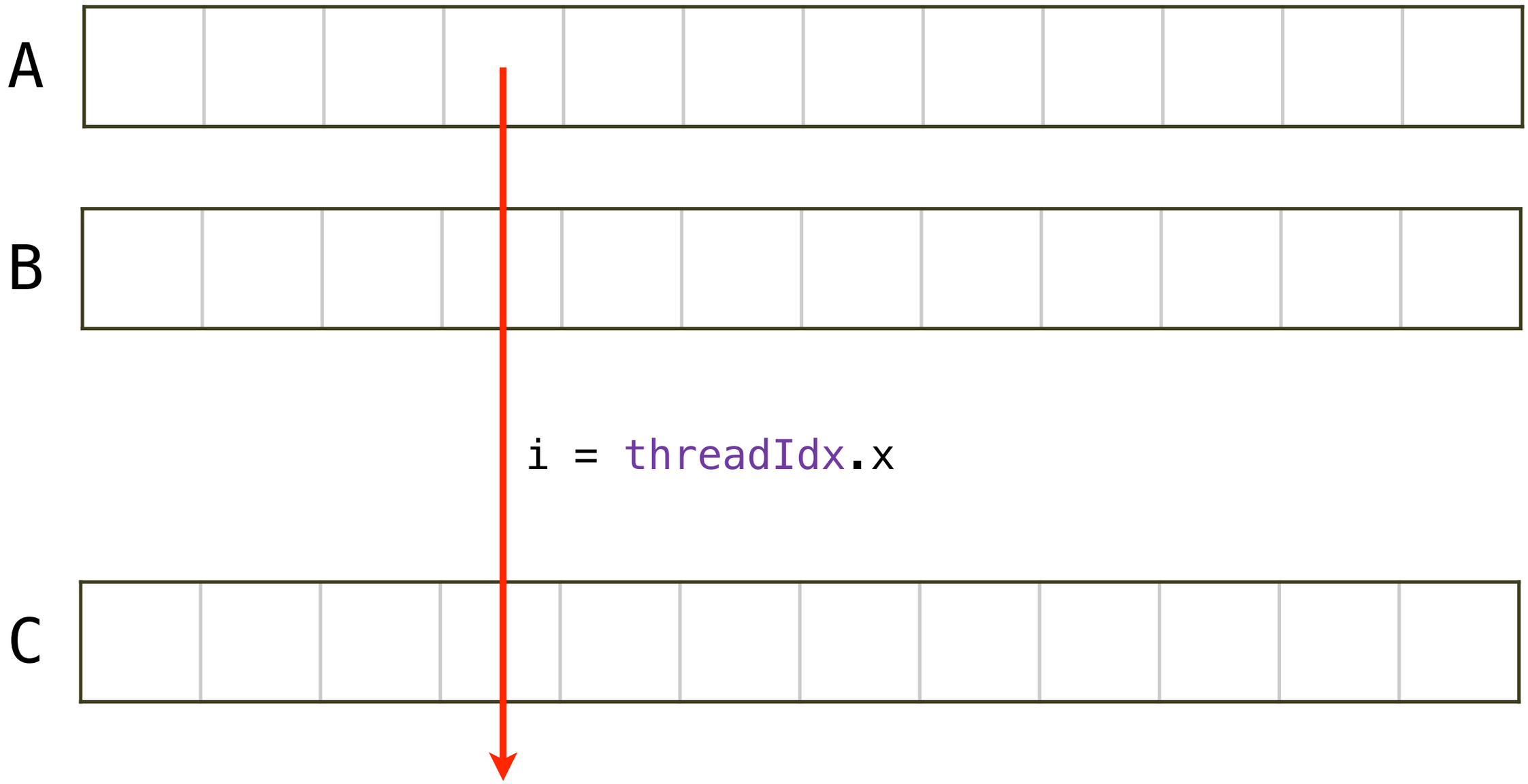

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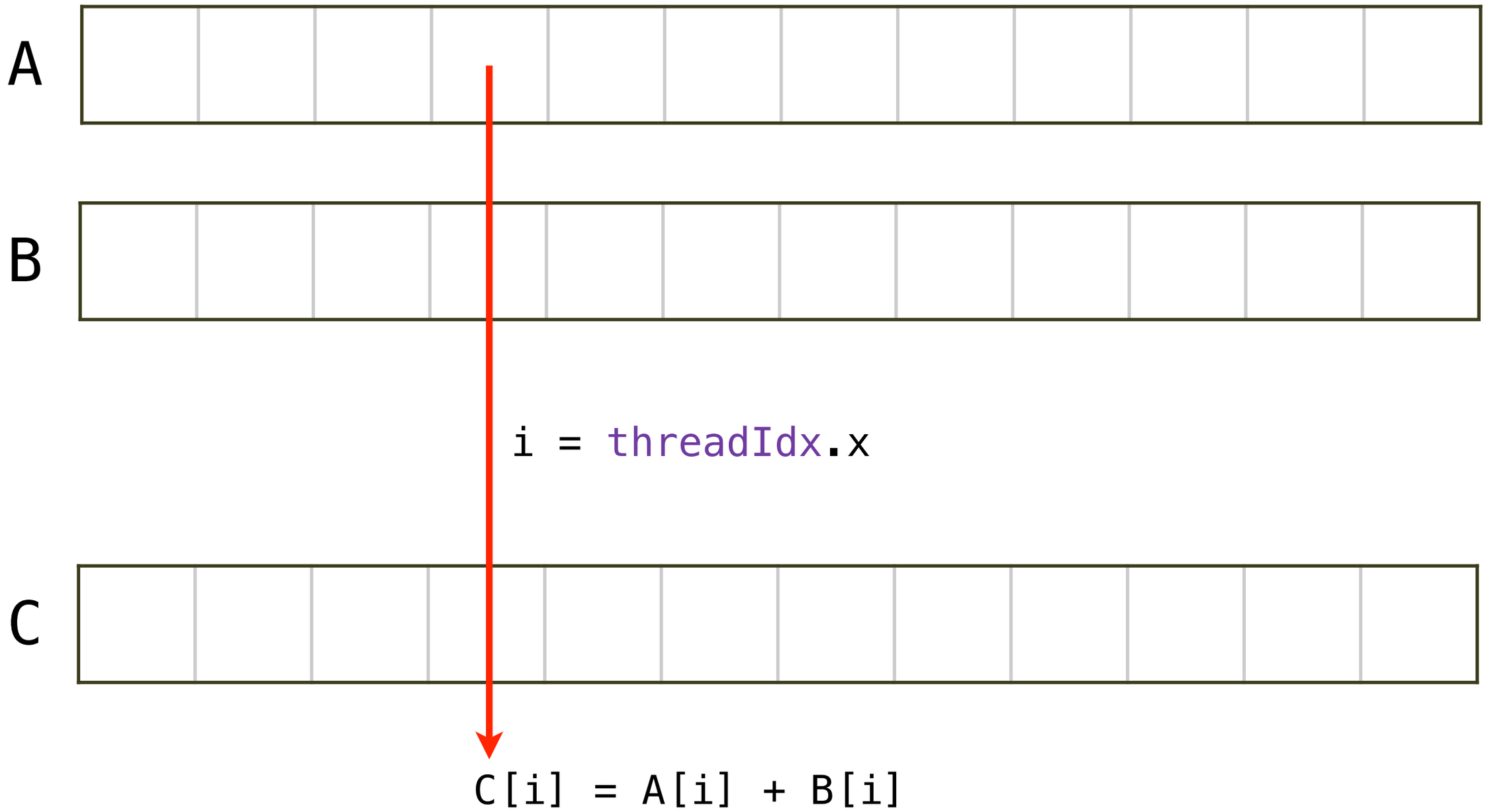

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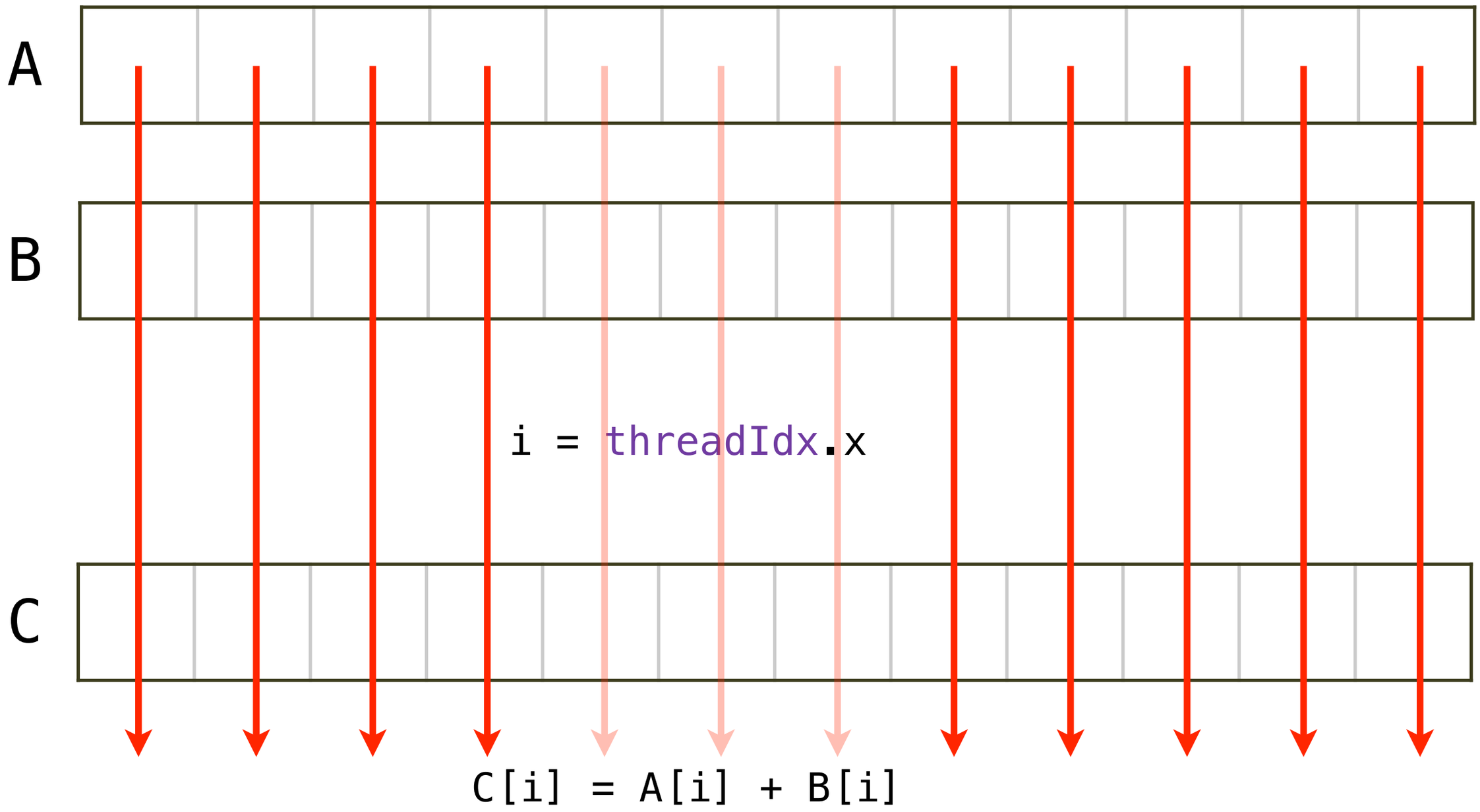

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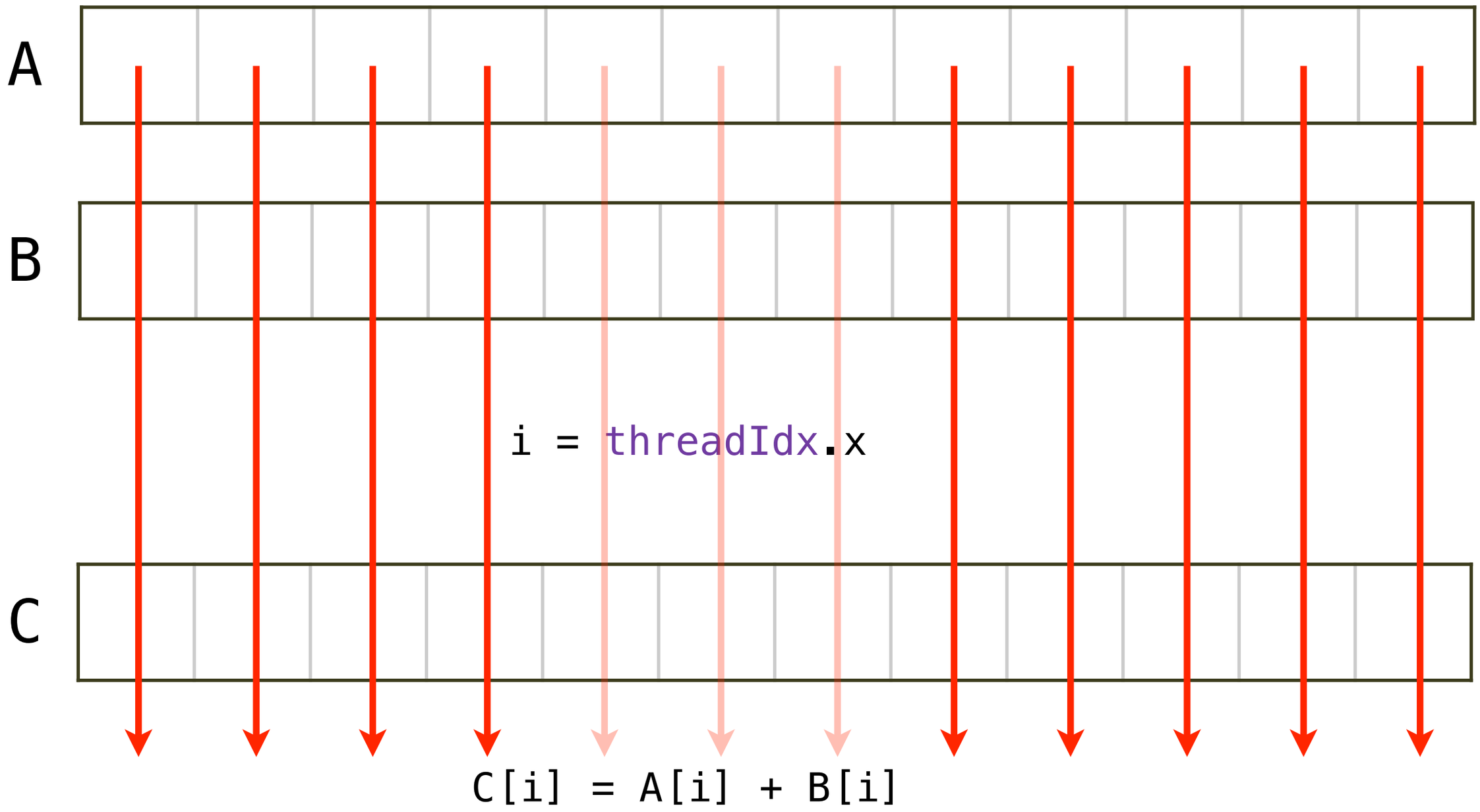


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VecAdd<<<1, N>>>(A, B, C);
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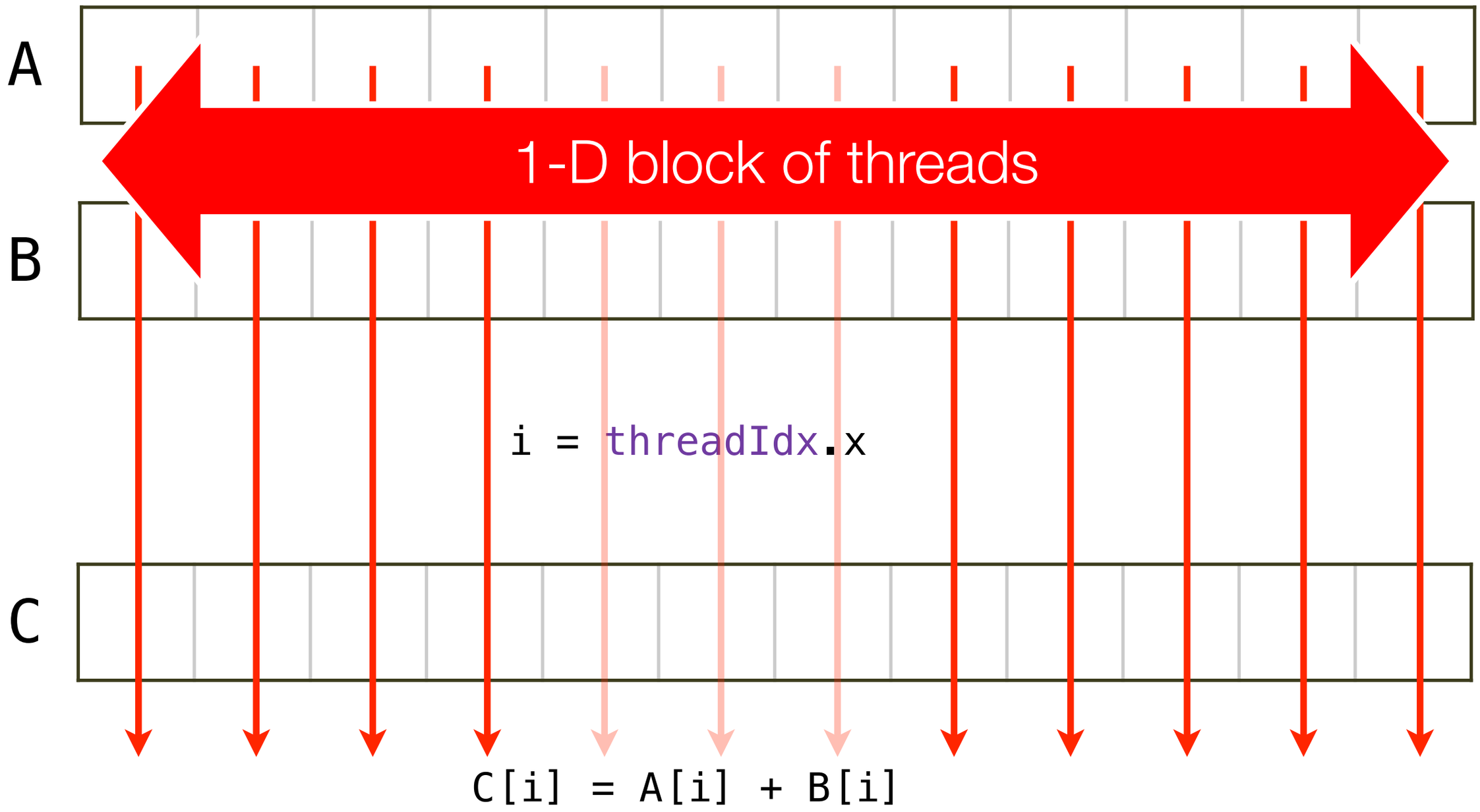


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What about branches?

Single control, multiple threads

Branching without Control

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Branching without Control

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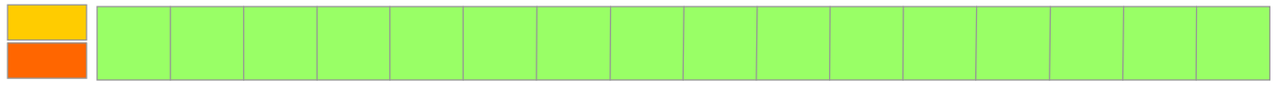

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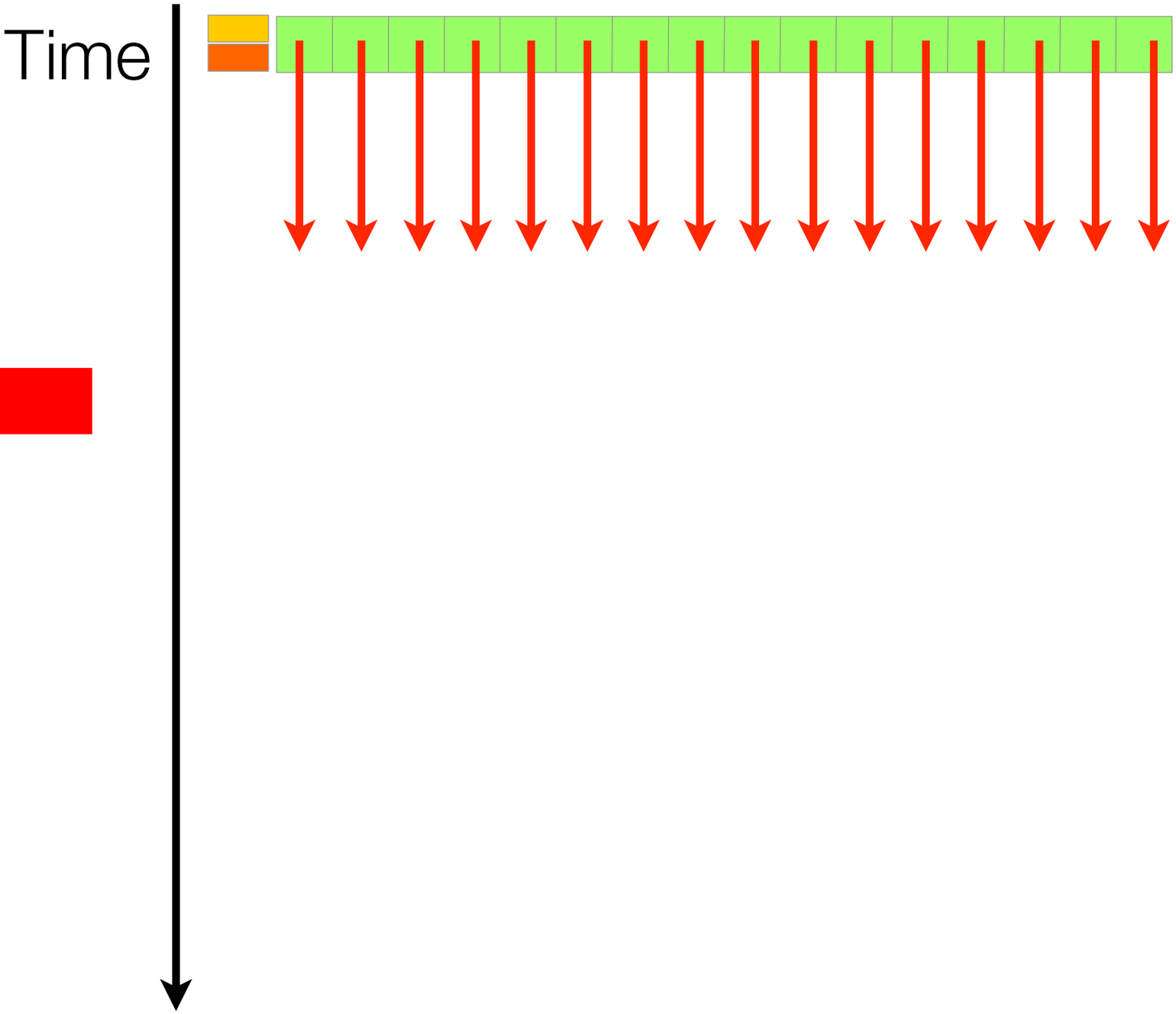


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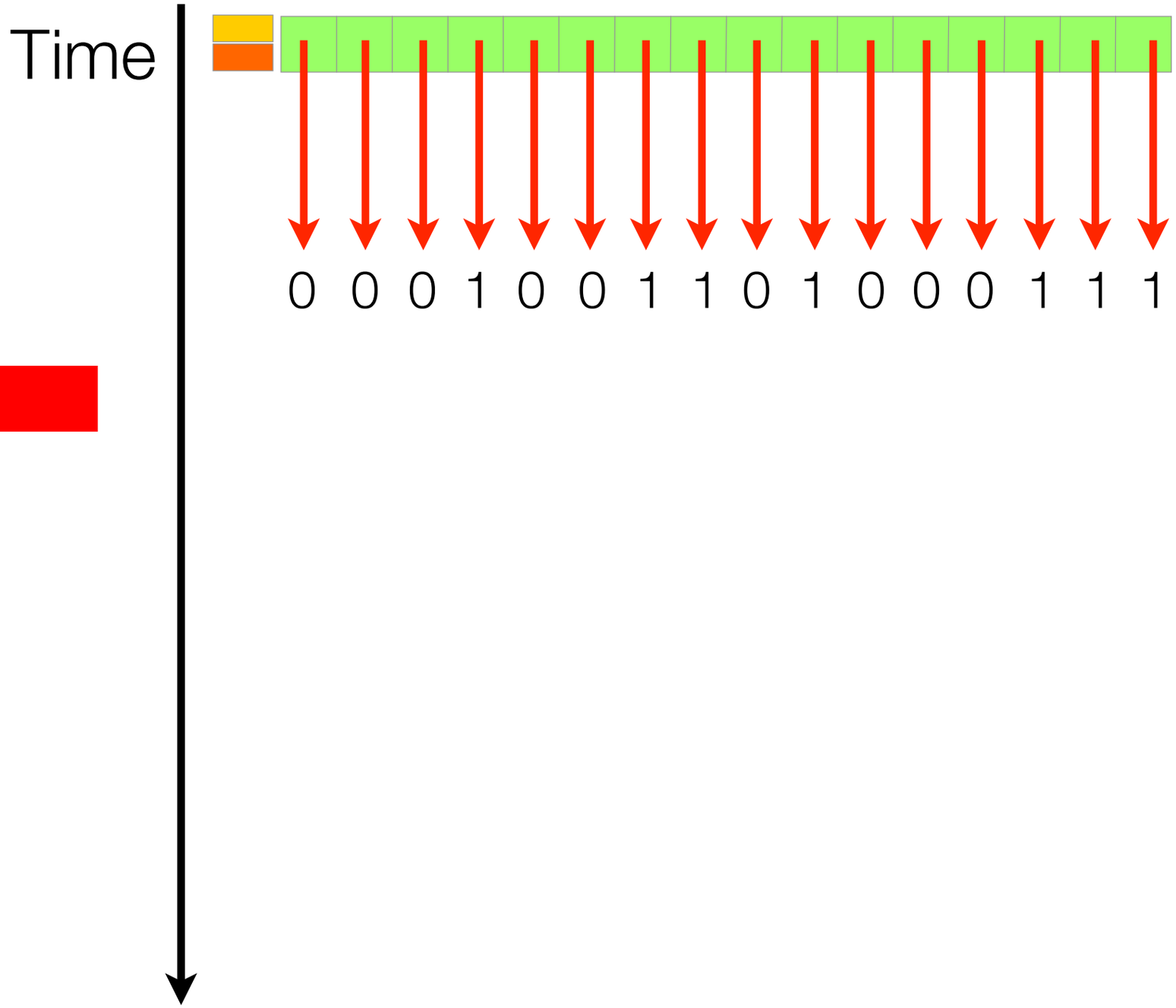

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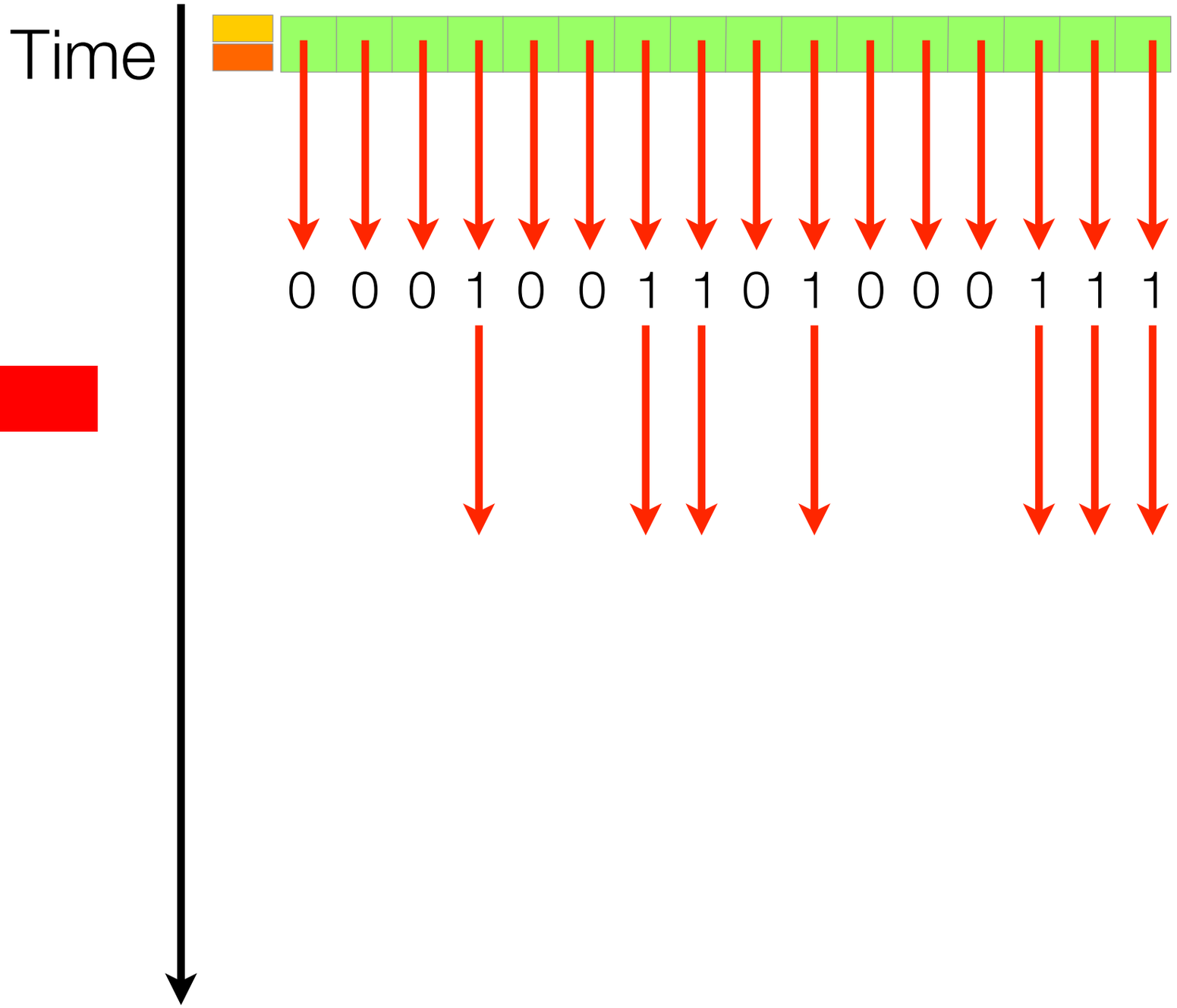

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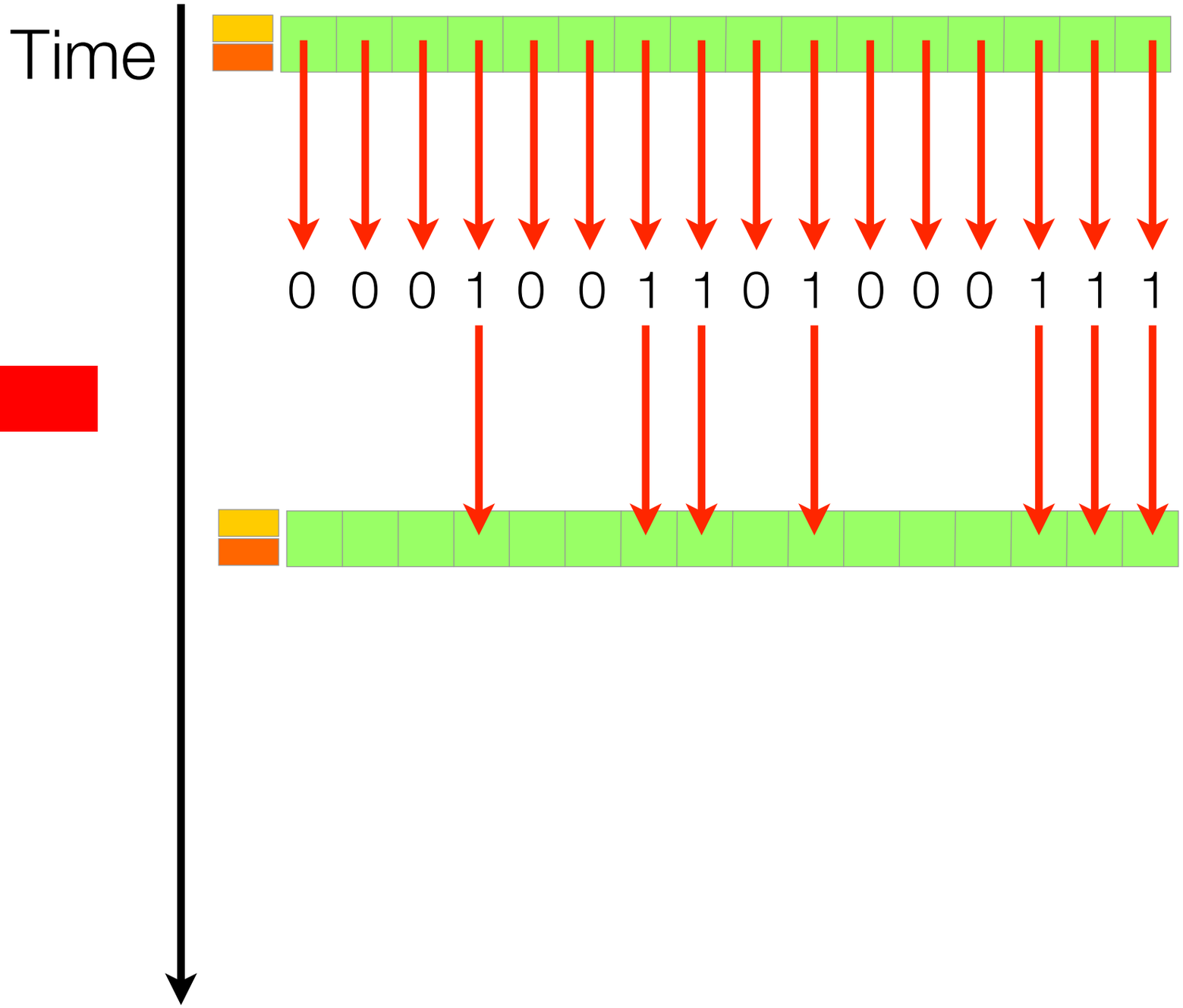

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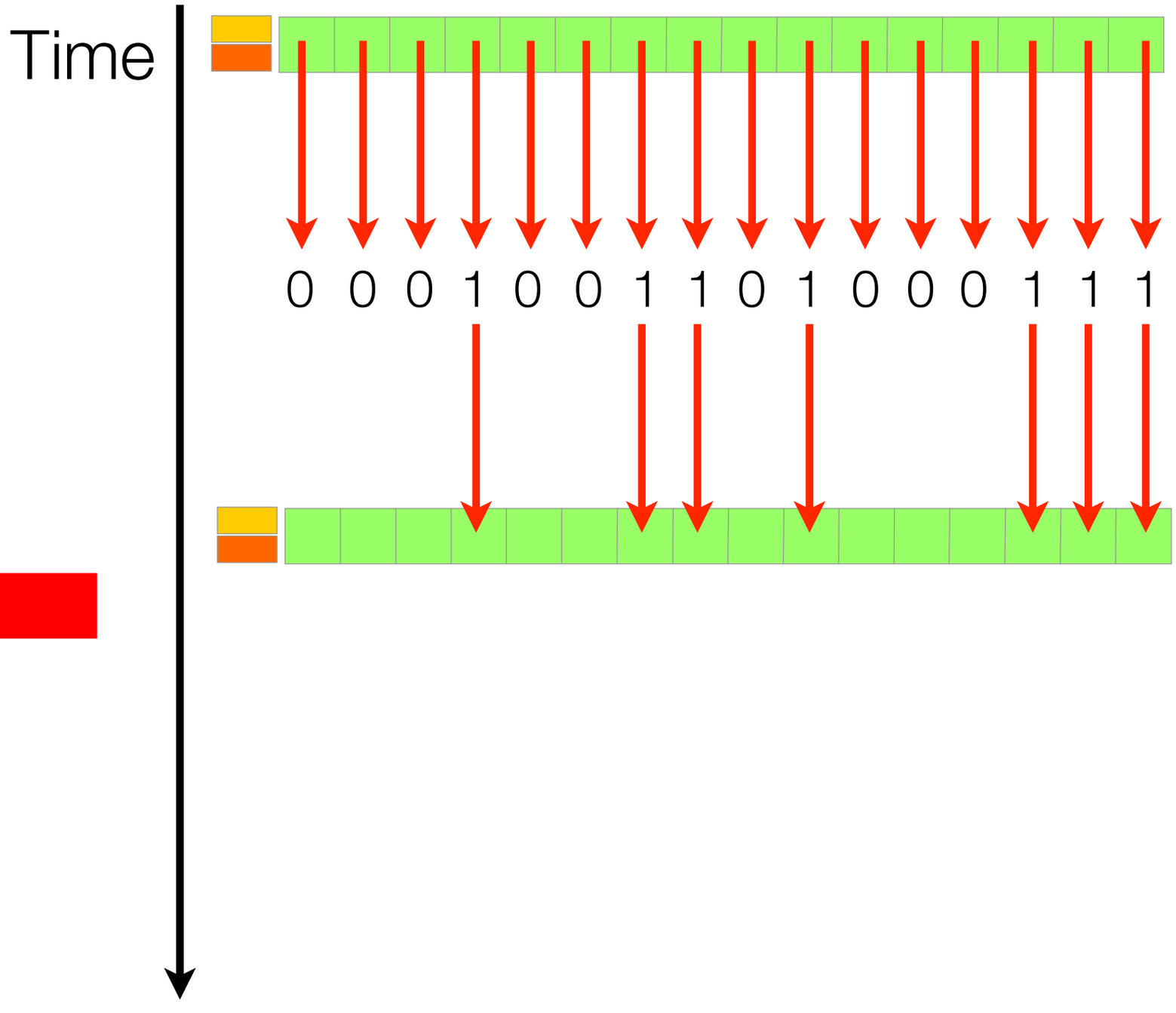

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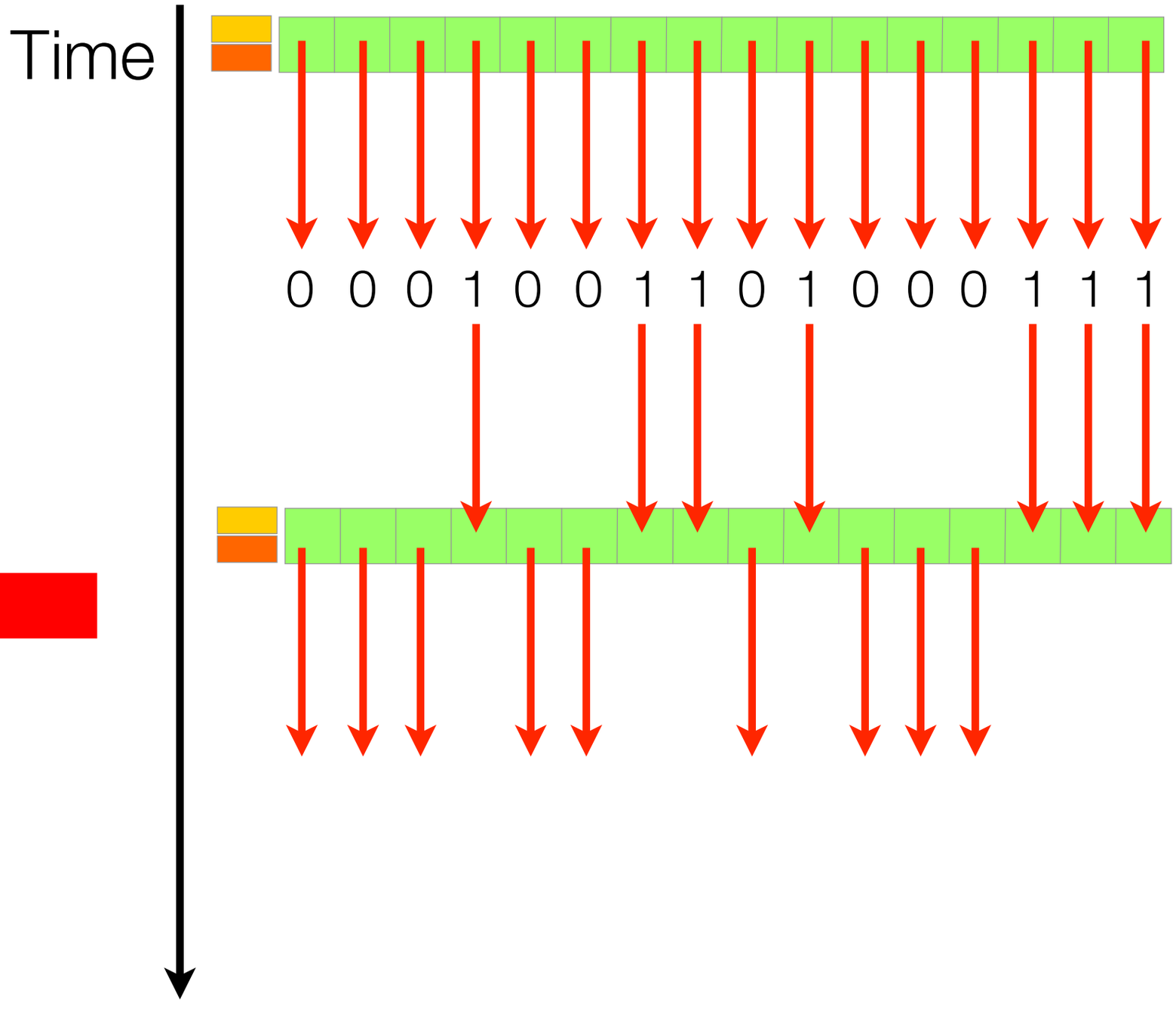

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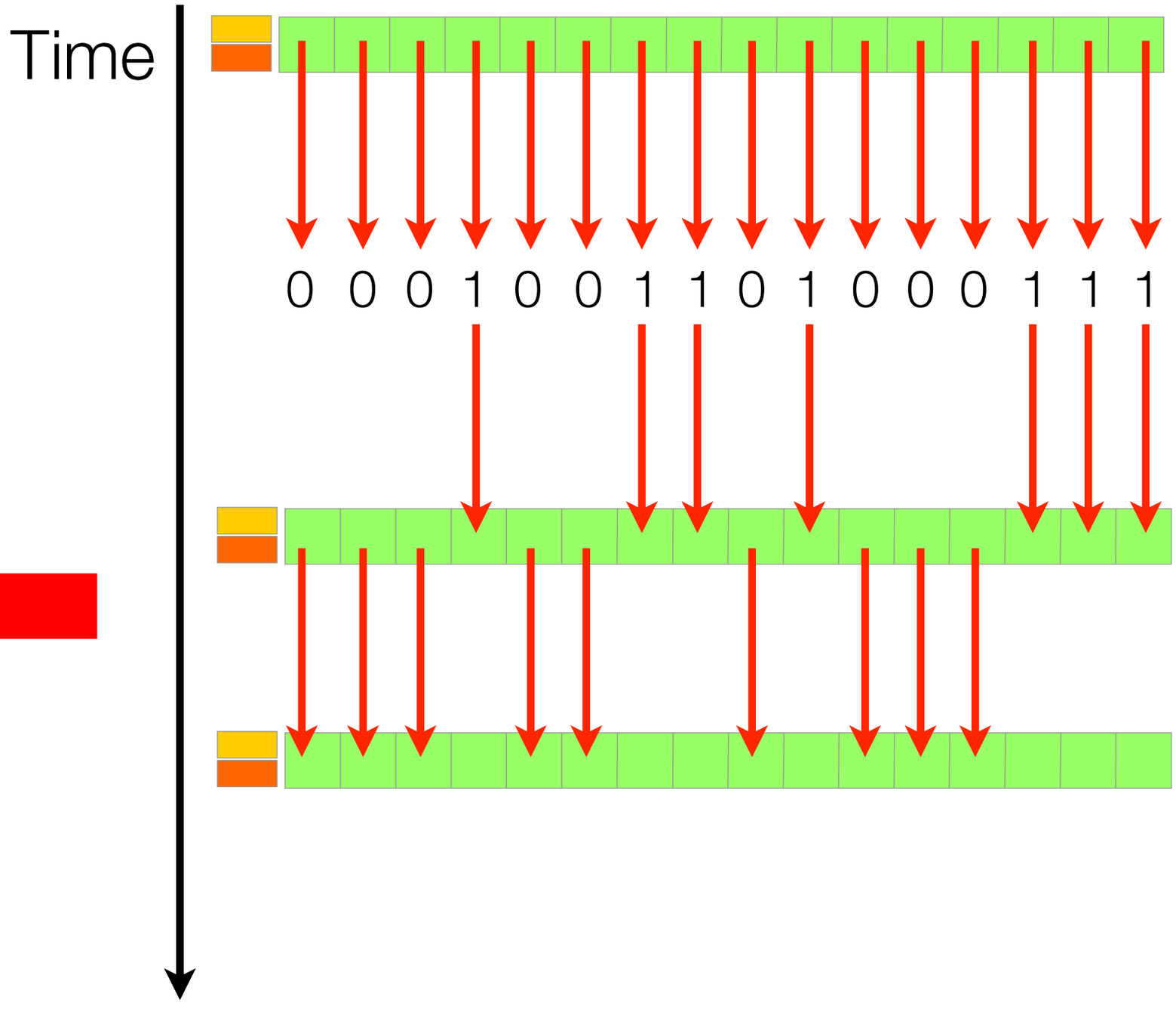

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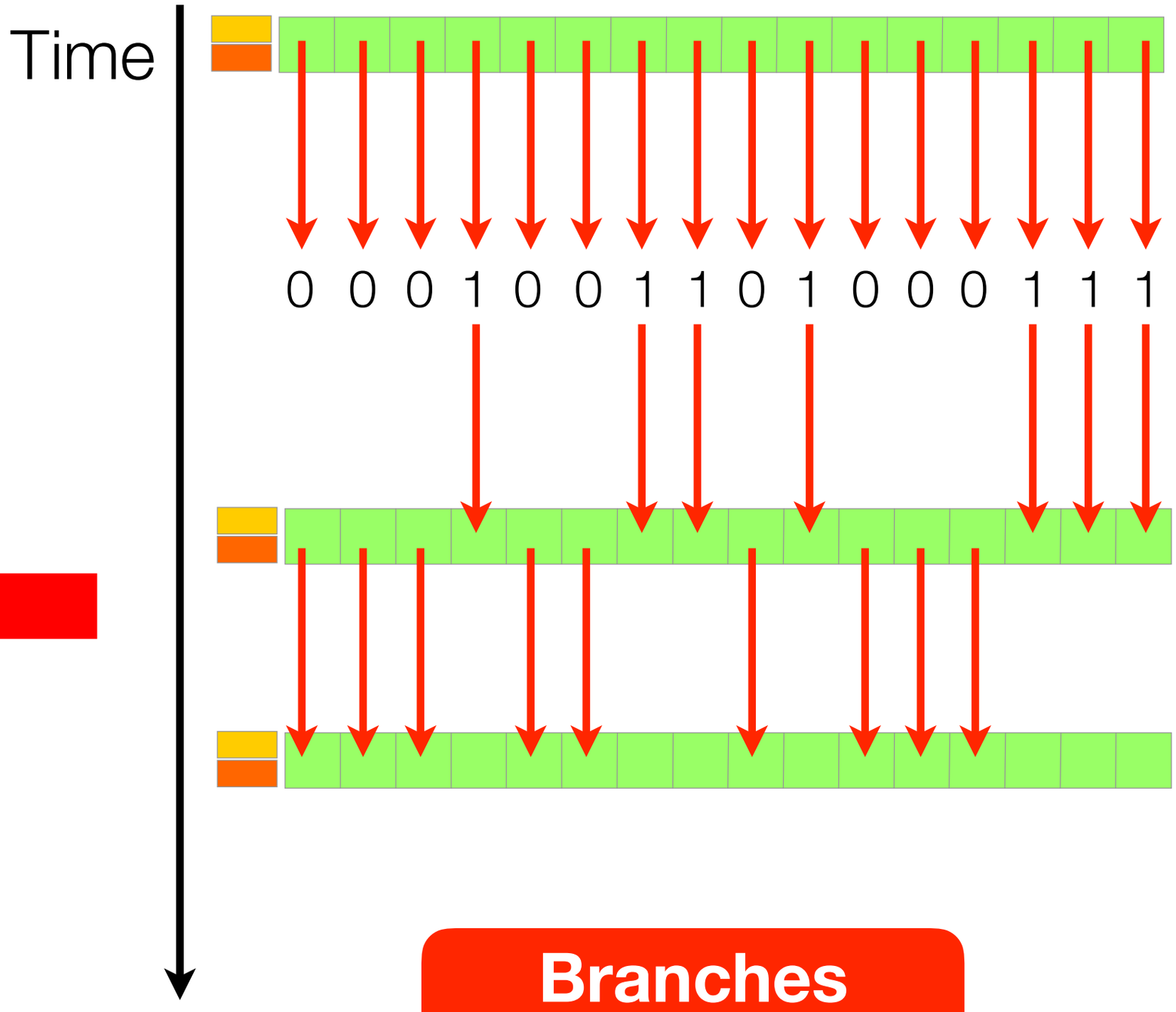

Branches produce stalls

Cache Effects

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- So, all these problems are ameliorated by the numbers

No Caching World

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Time

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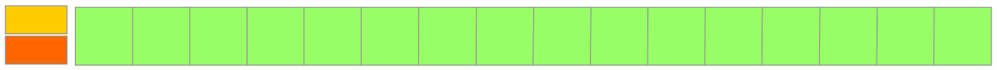

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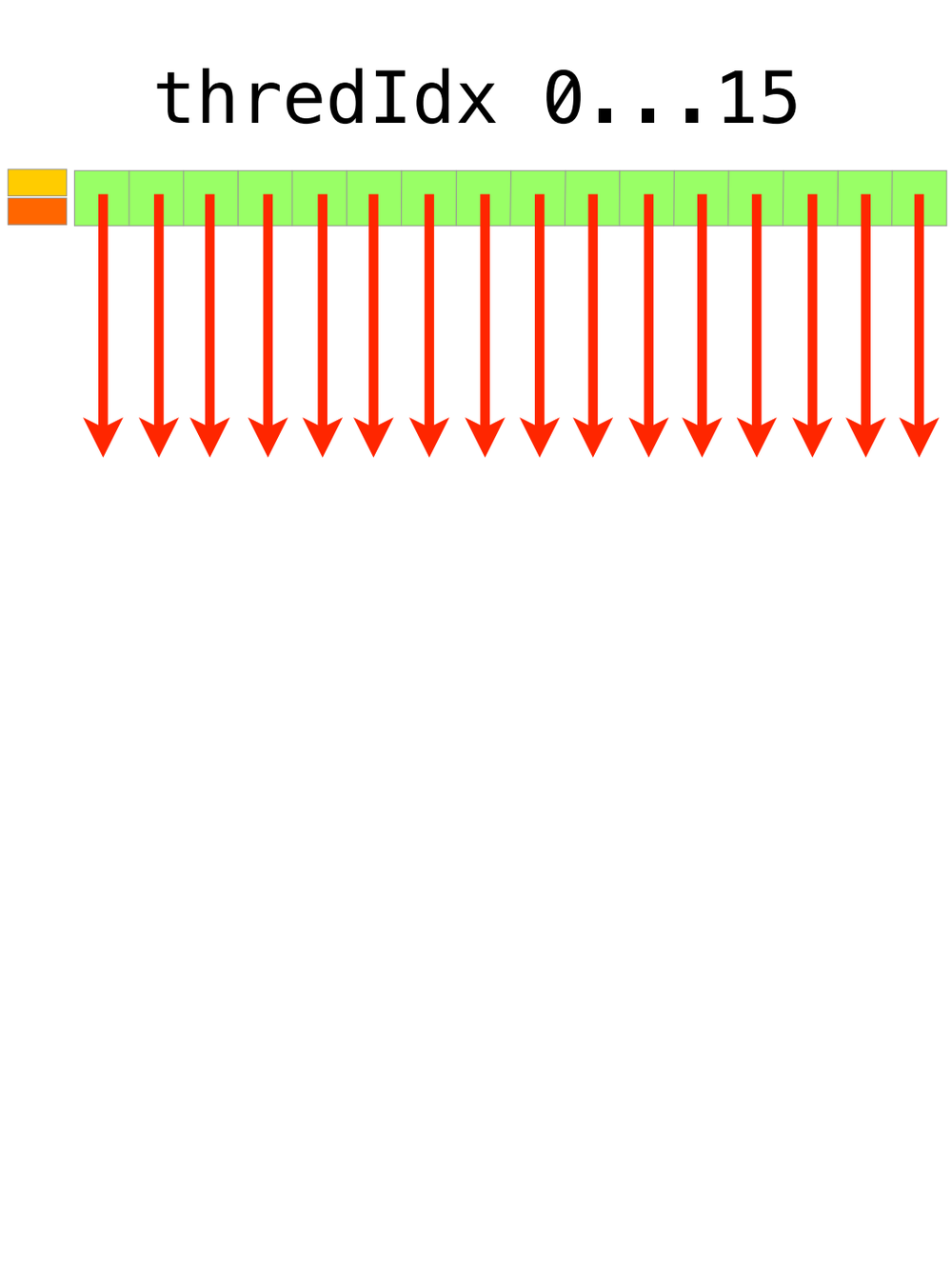

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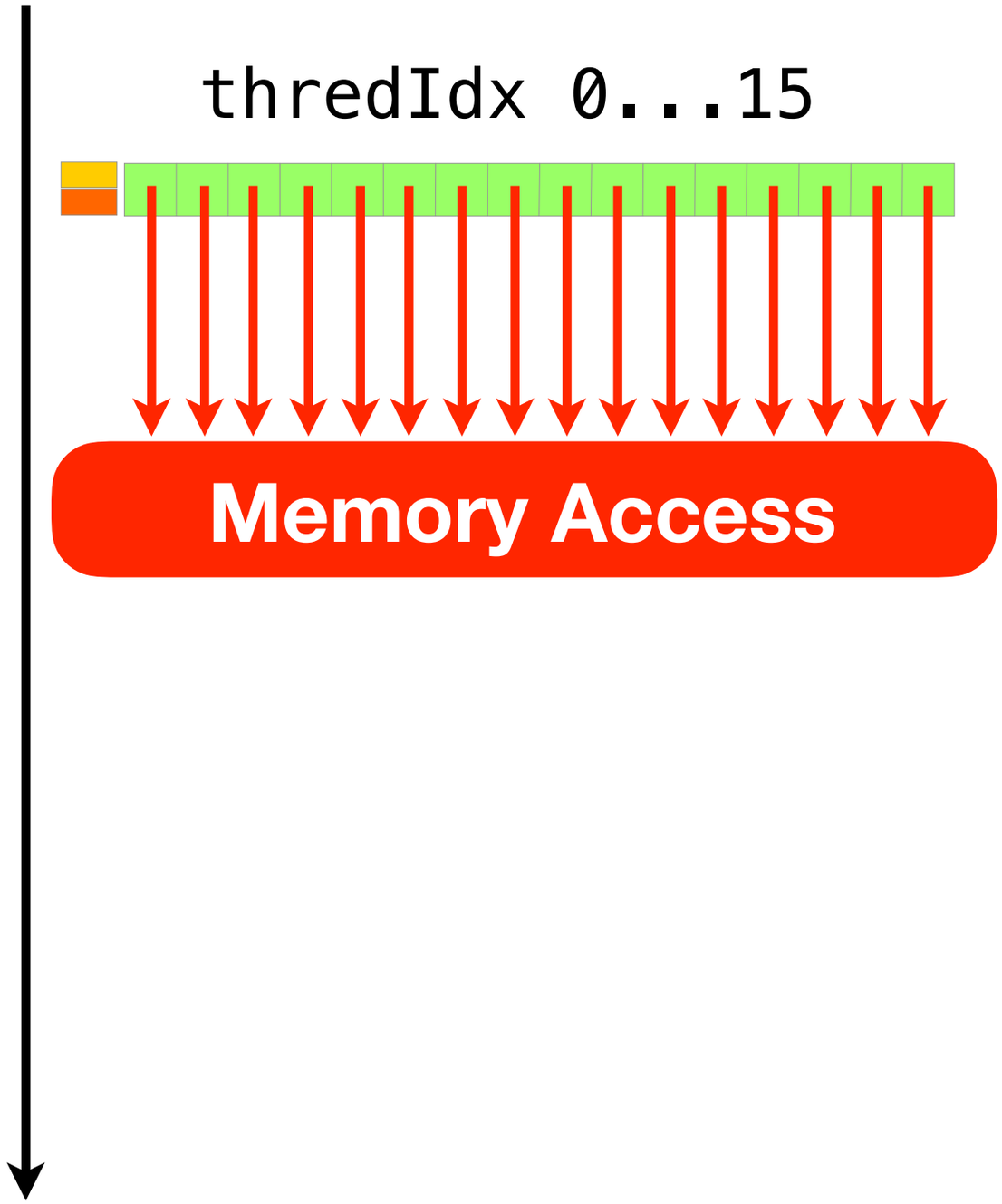

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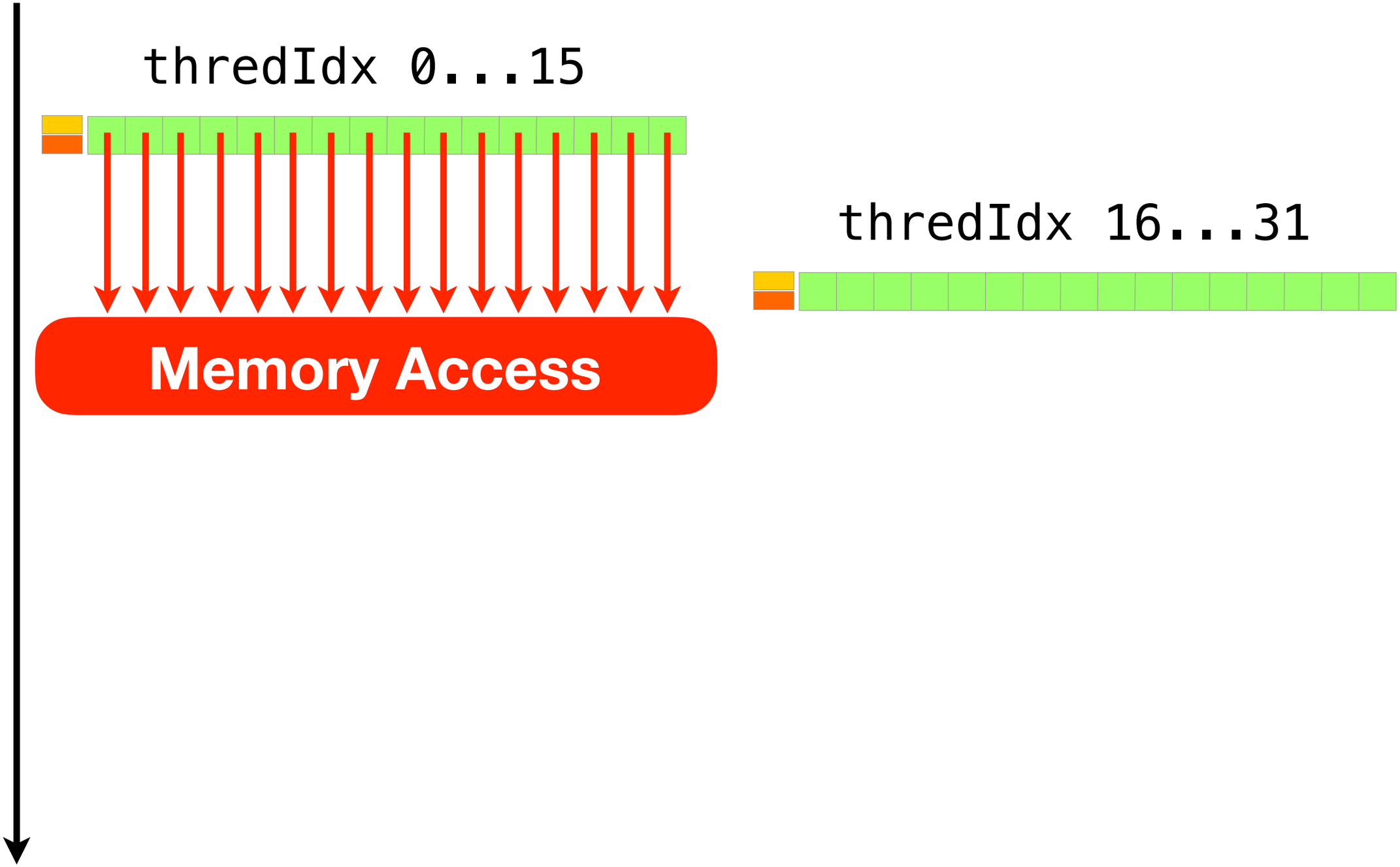

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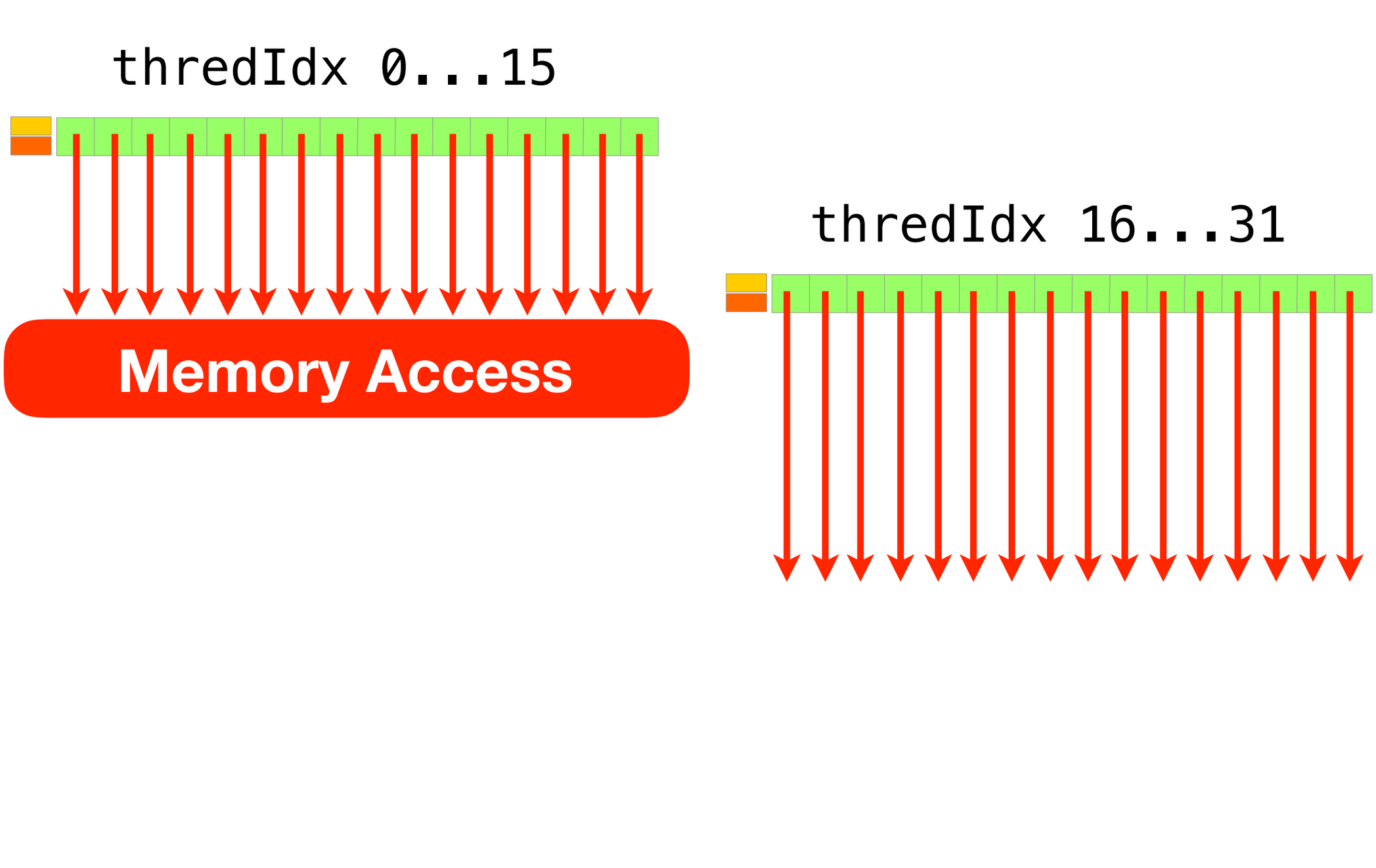

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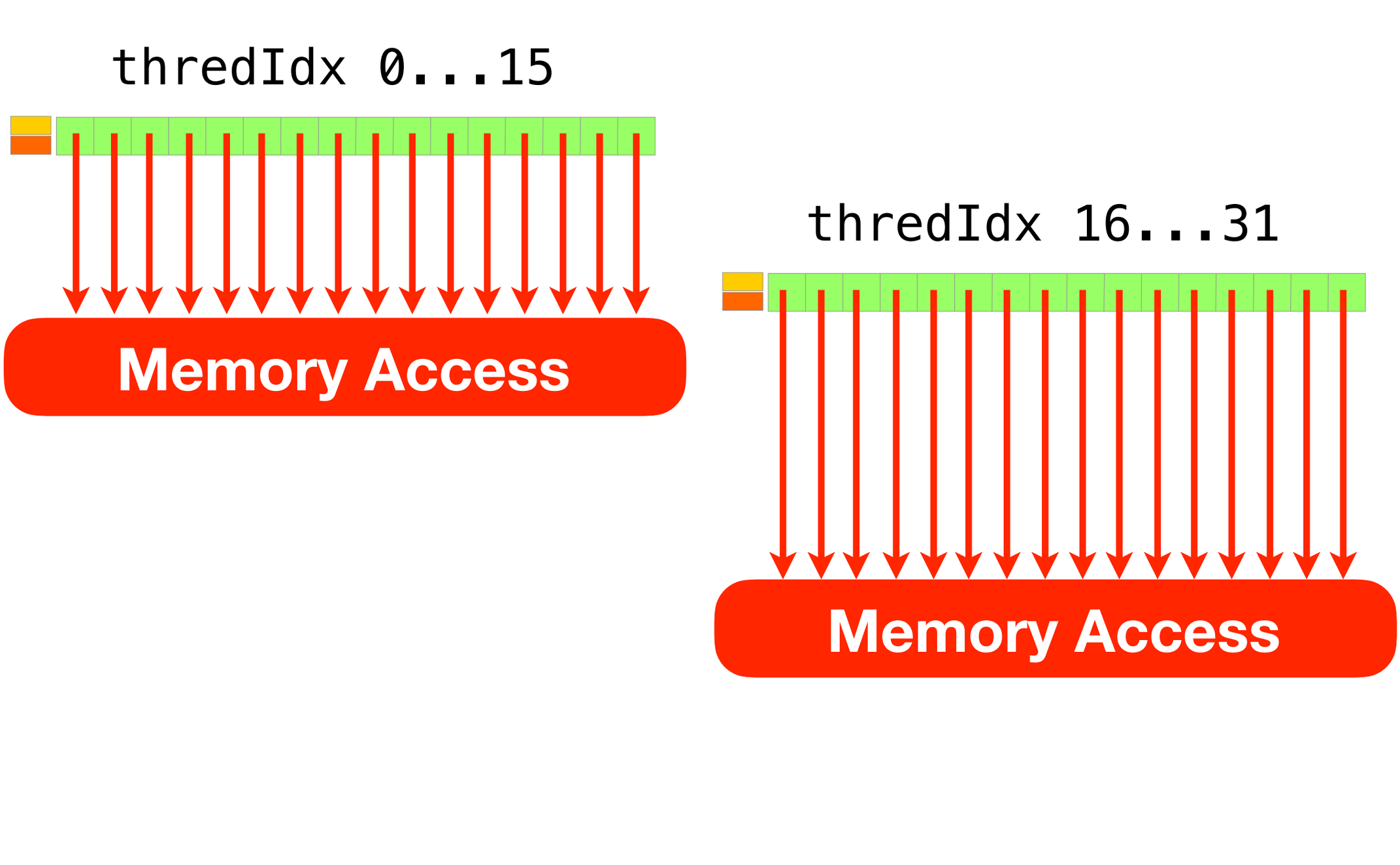

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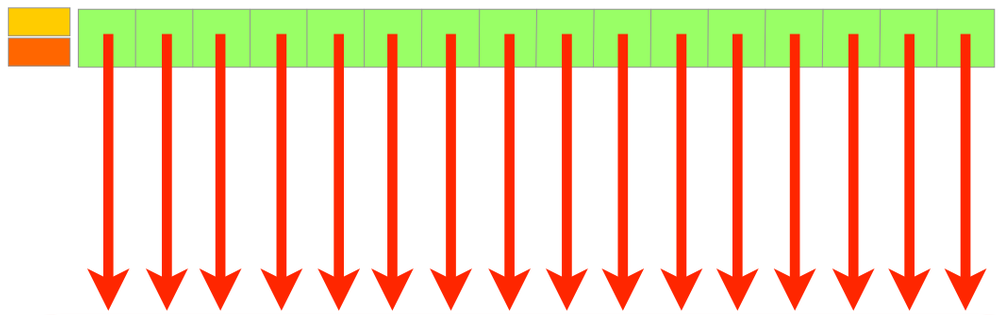
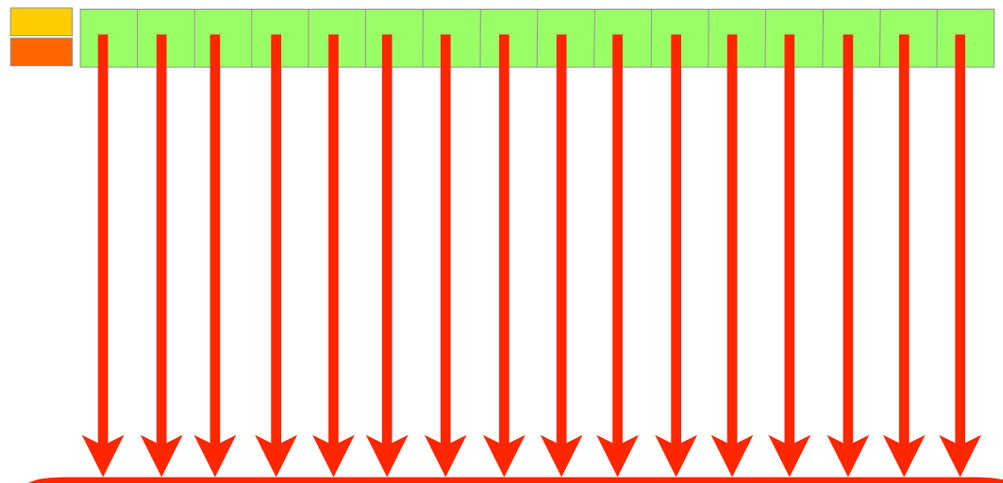
Time

thredIdx 0...15



Memory Access

thredIdx 16...31



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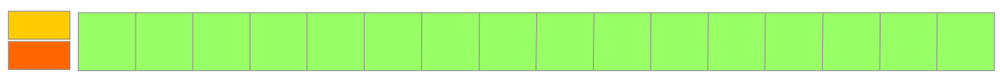

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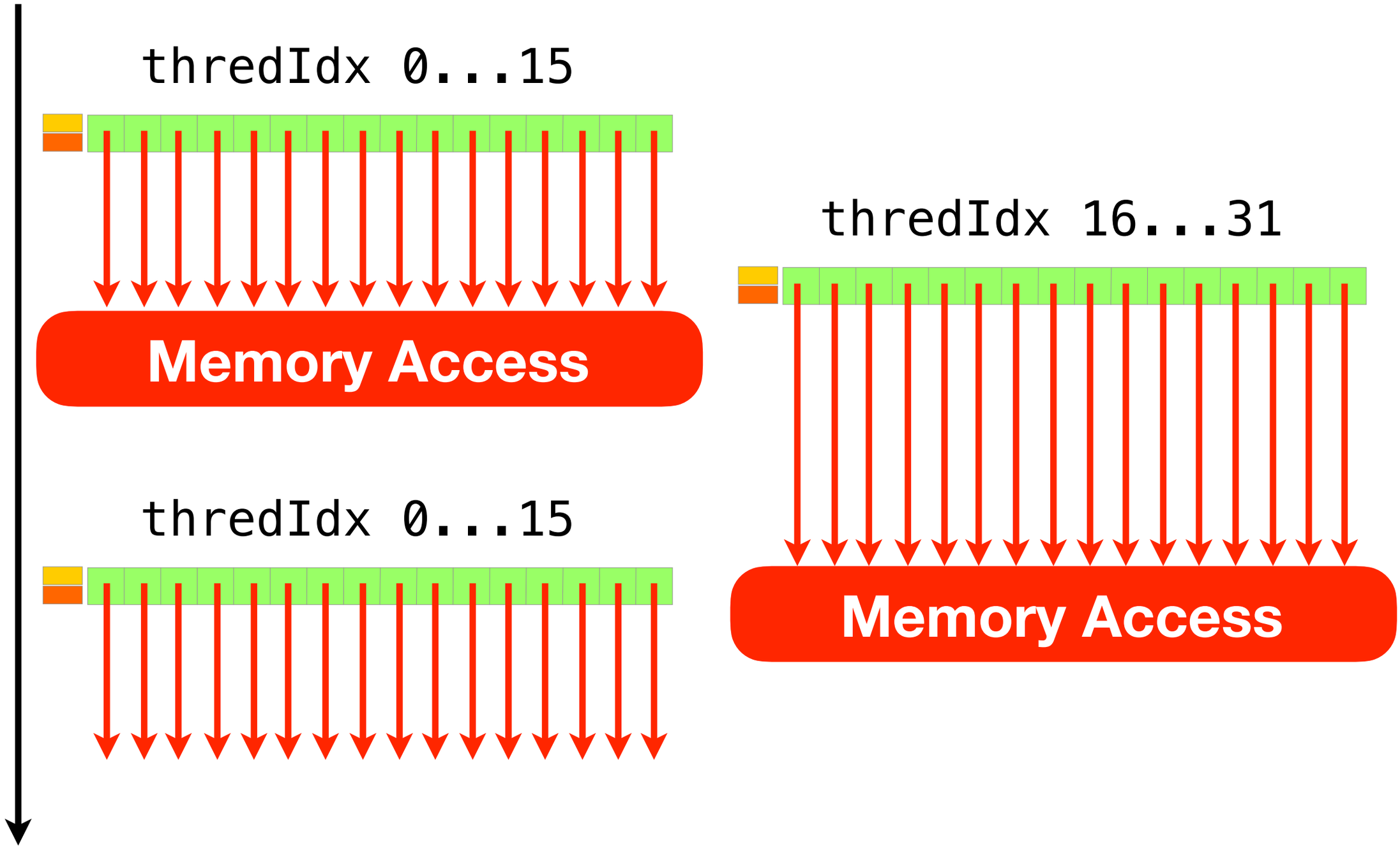
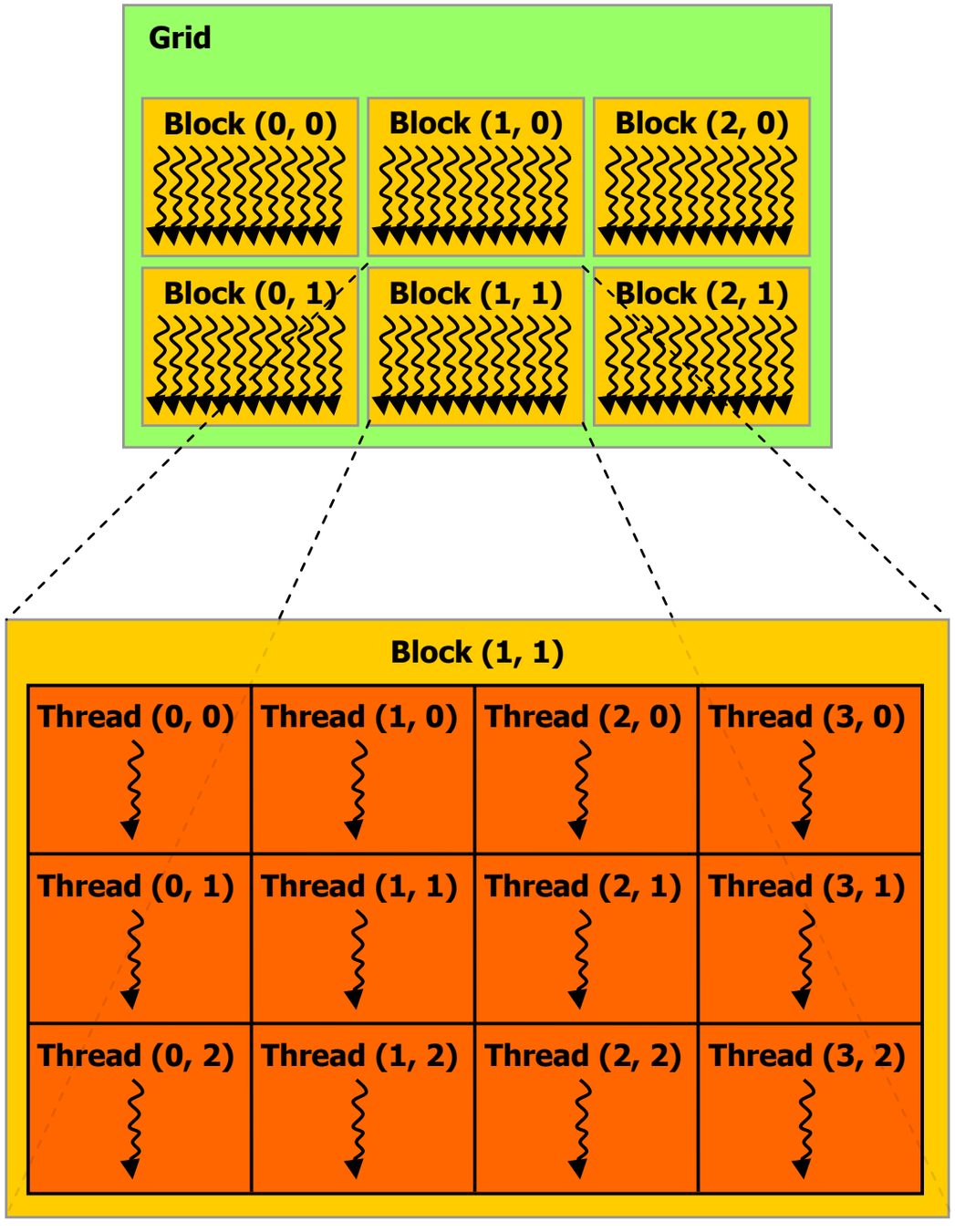


Thread Blocks



Memory Model

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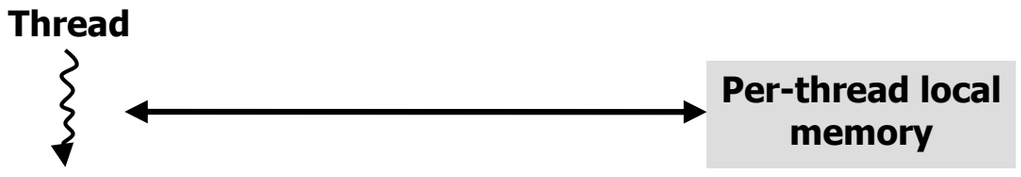

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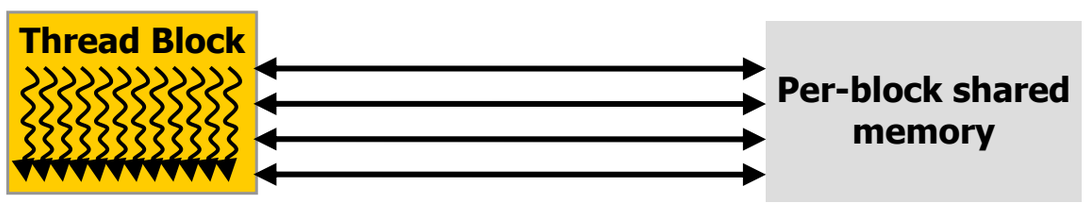

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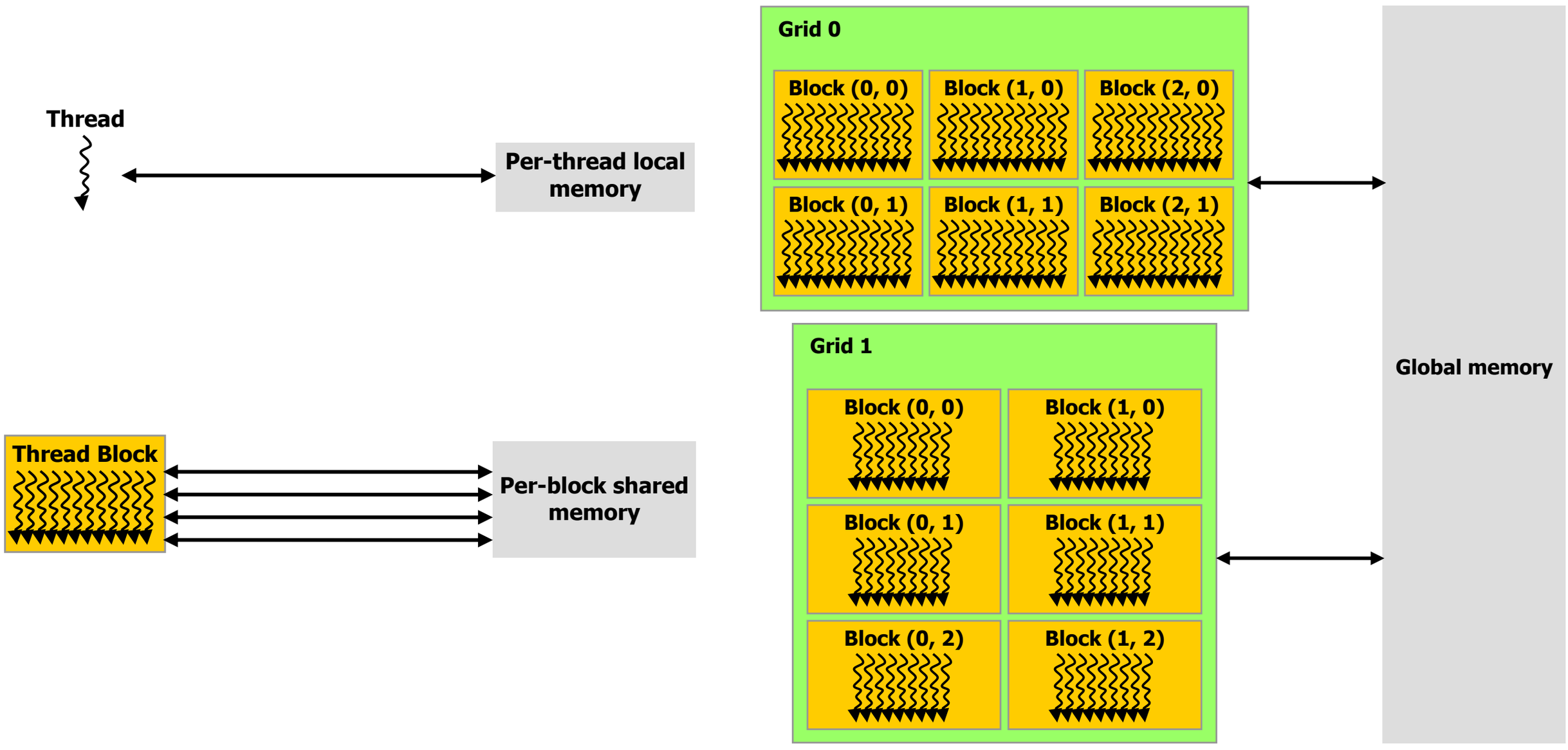

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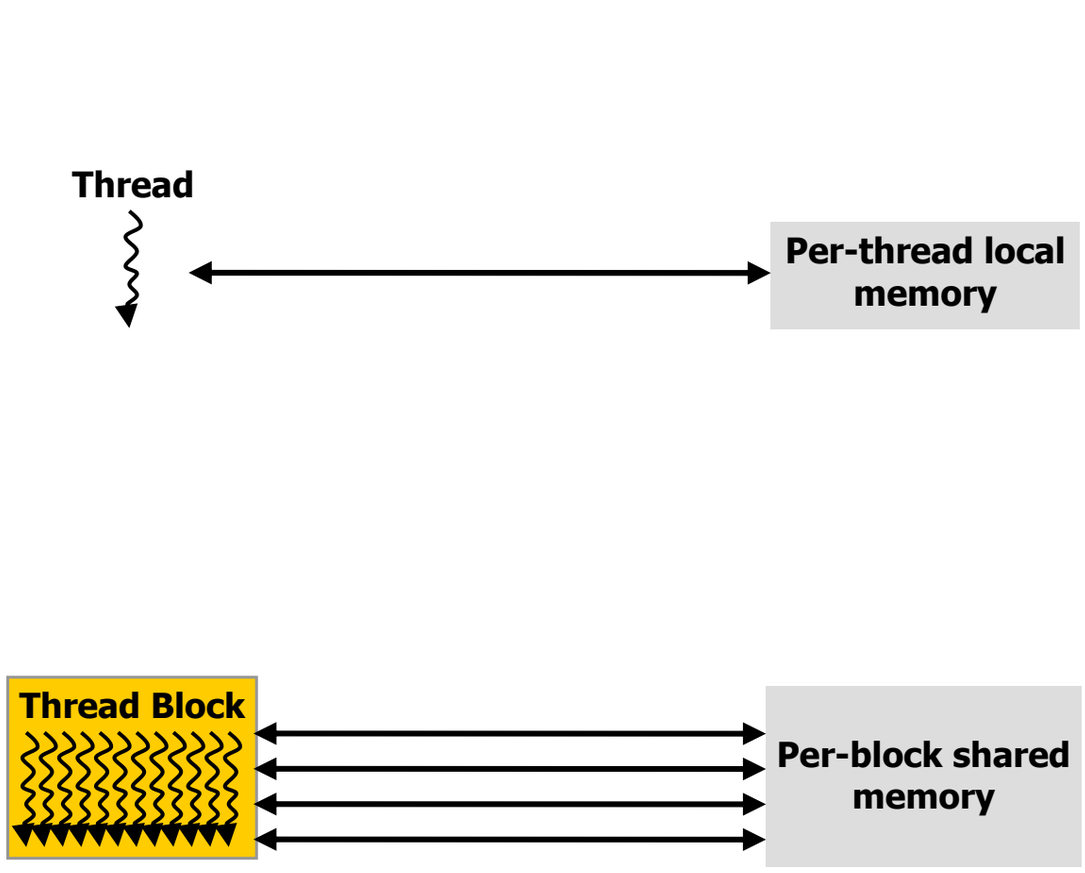

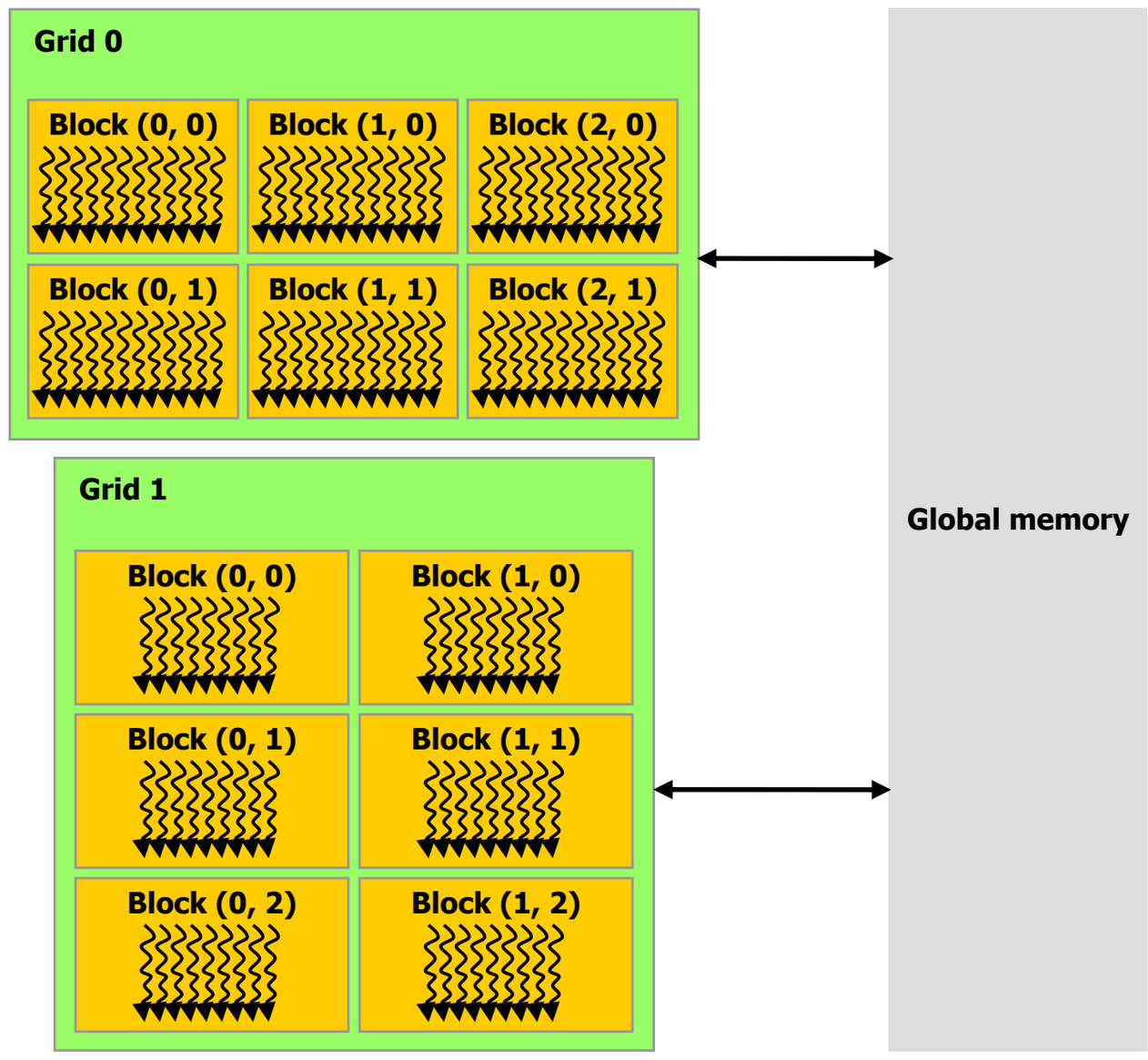

In Nvidia's jargon, 32 threads are called a *warp*

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- Blocks can be arranged in arrays or grids, as developers see suitable for their case

Blocks and Warps: Scheduling

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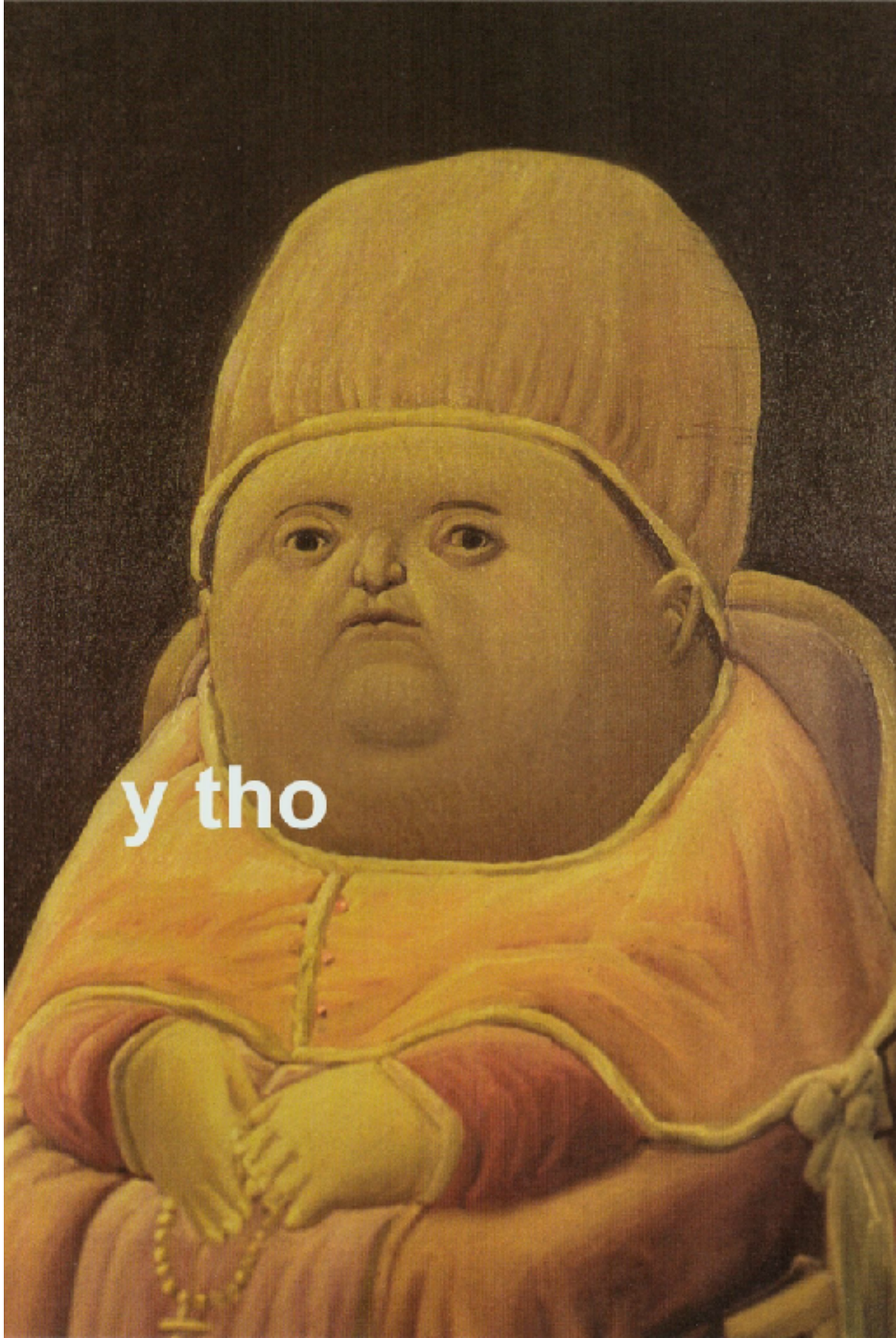
Jobs with CUDA



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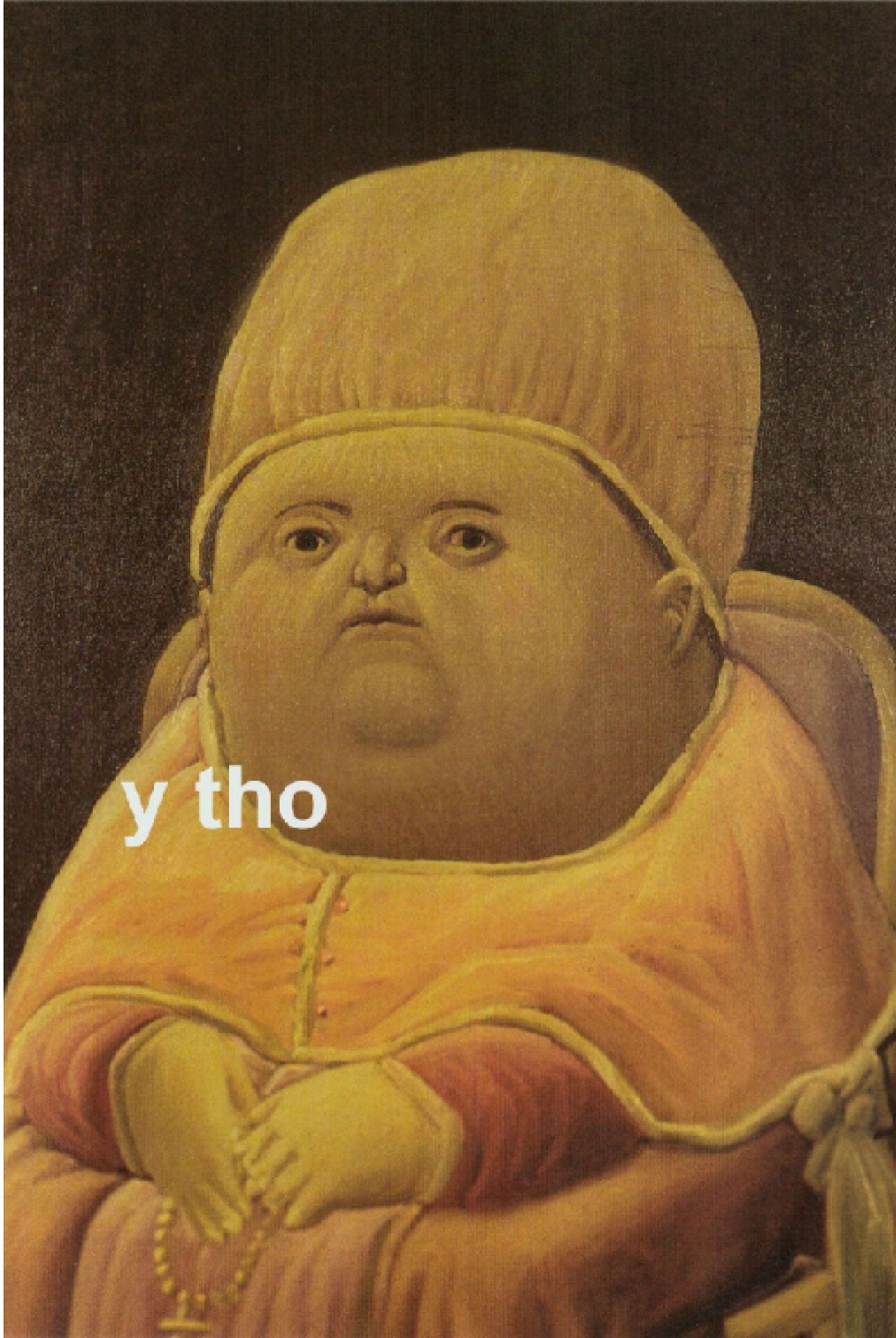
- Physics and Graphics



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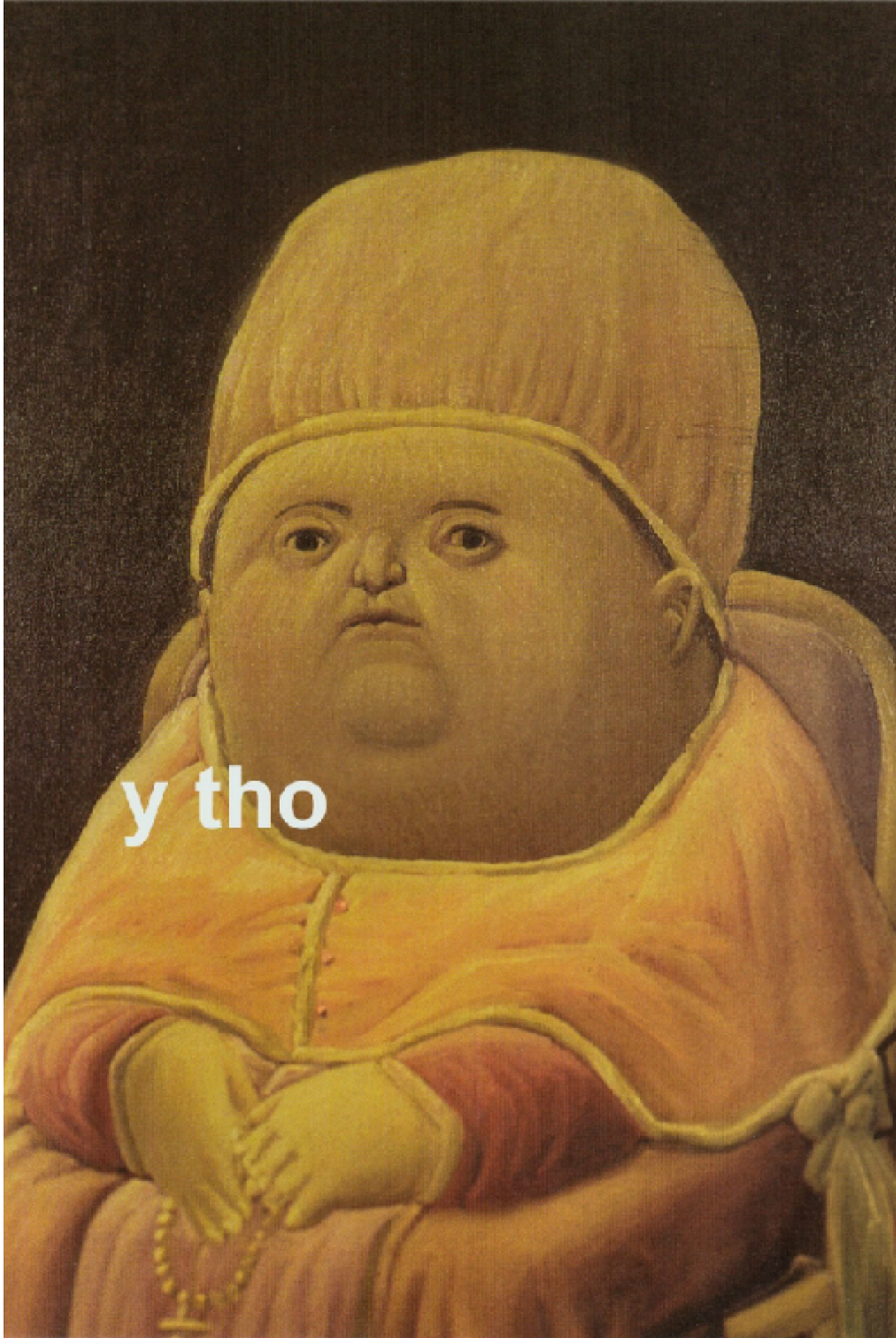

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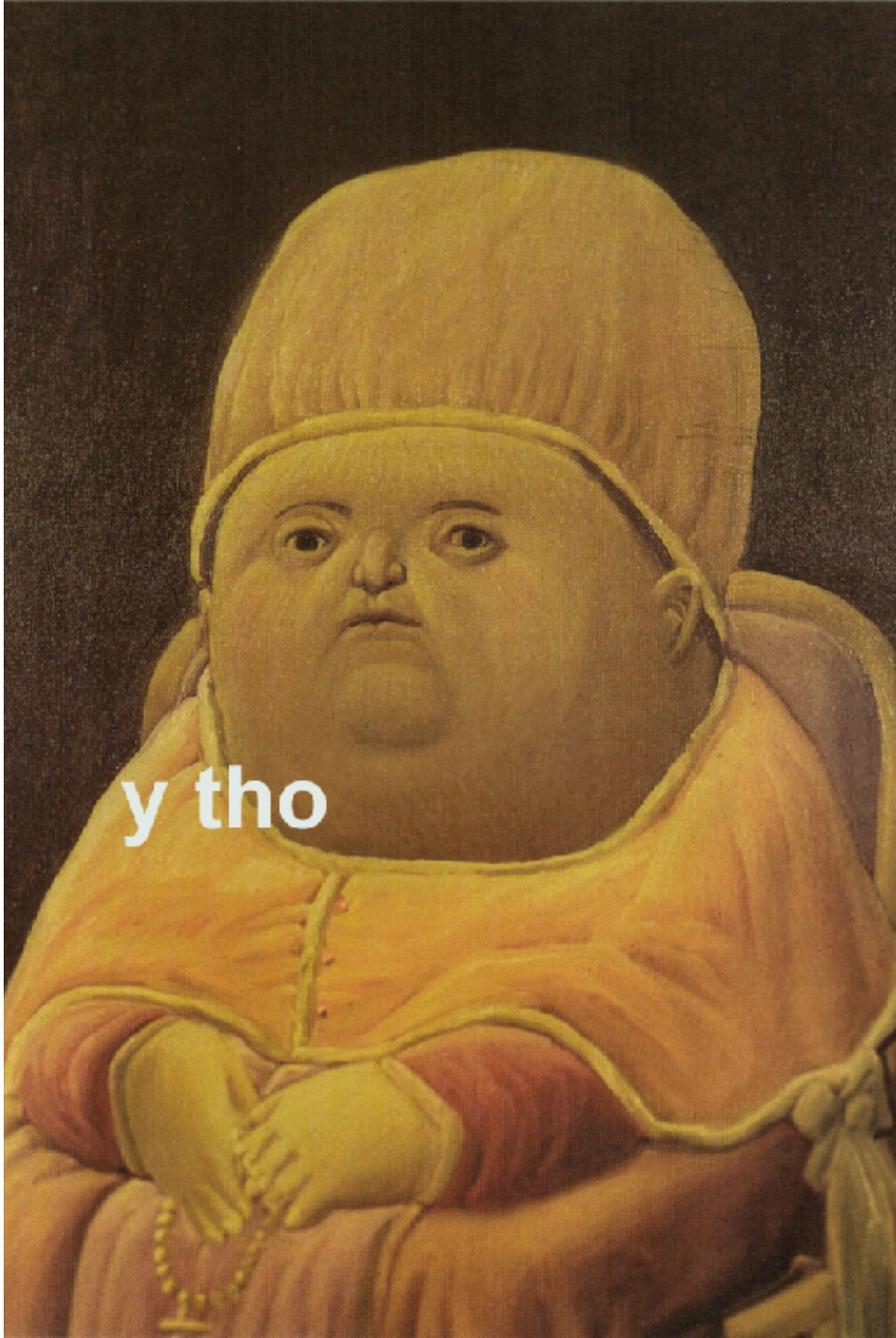

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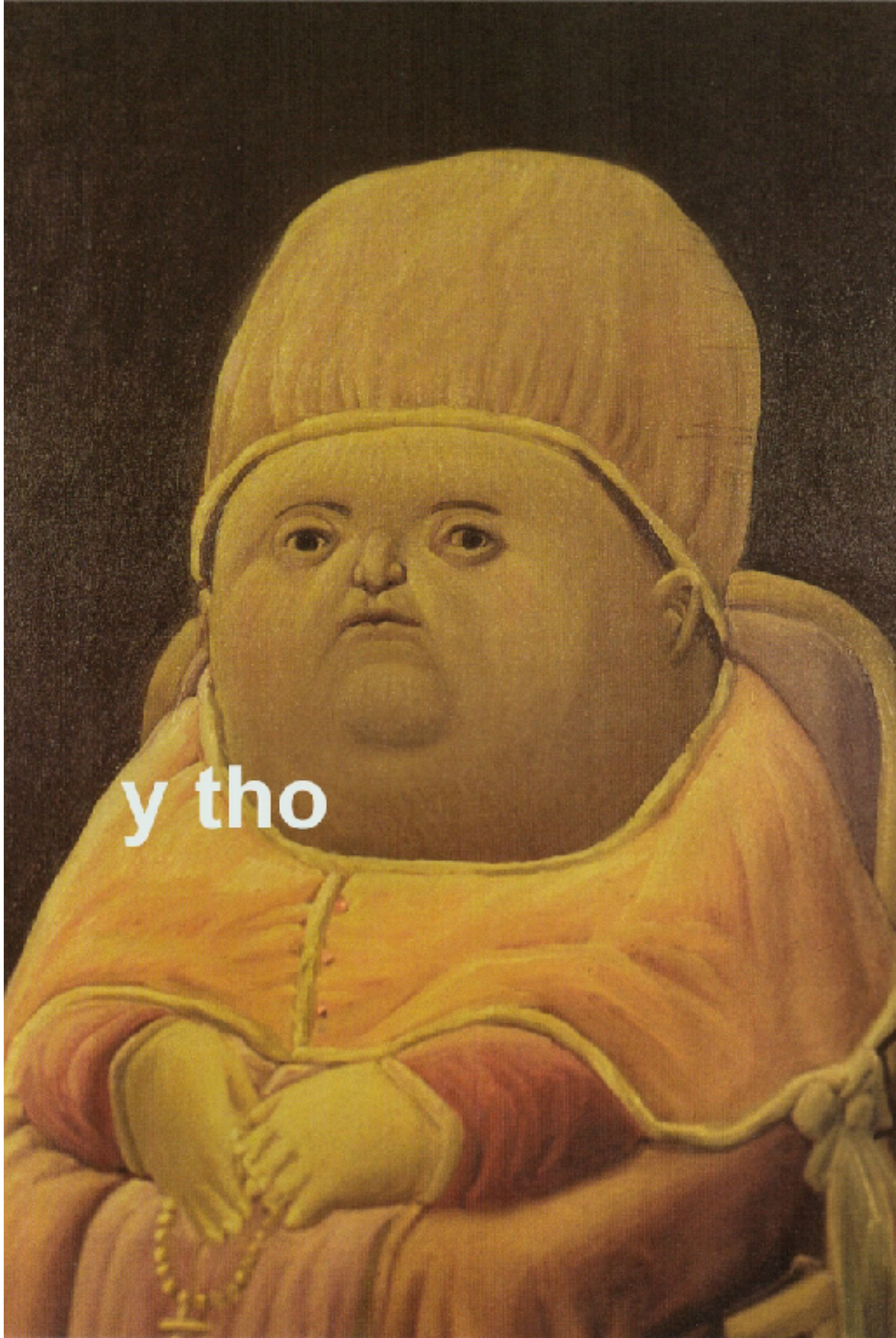

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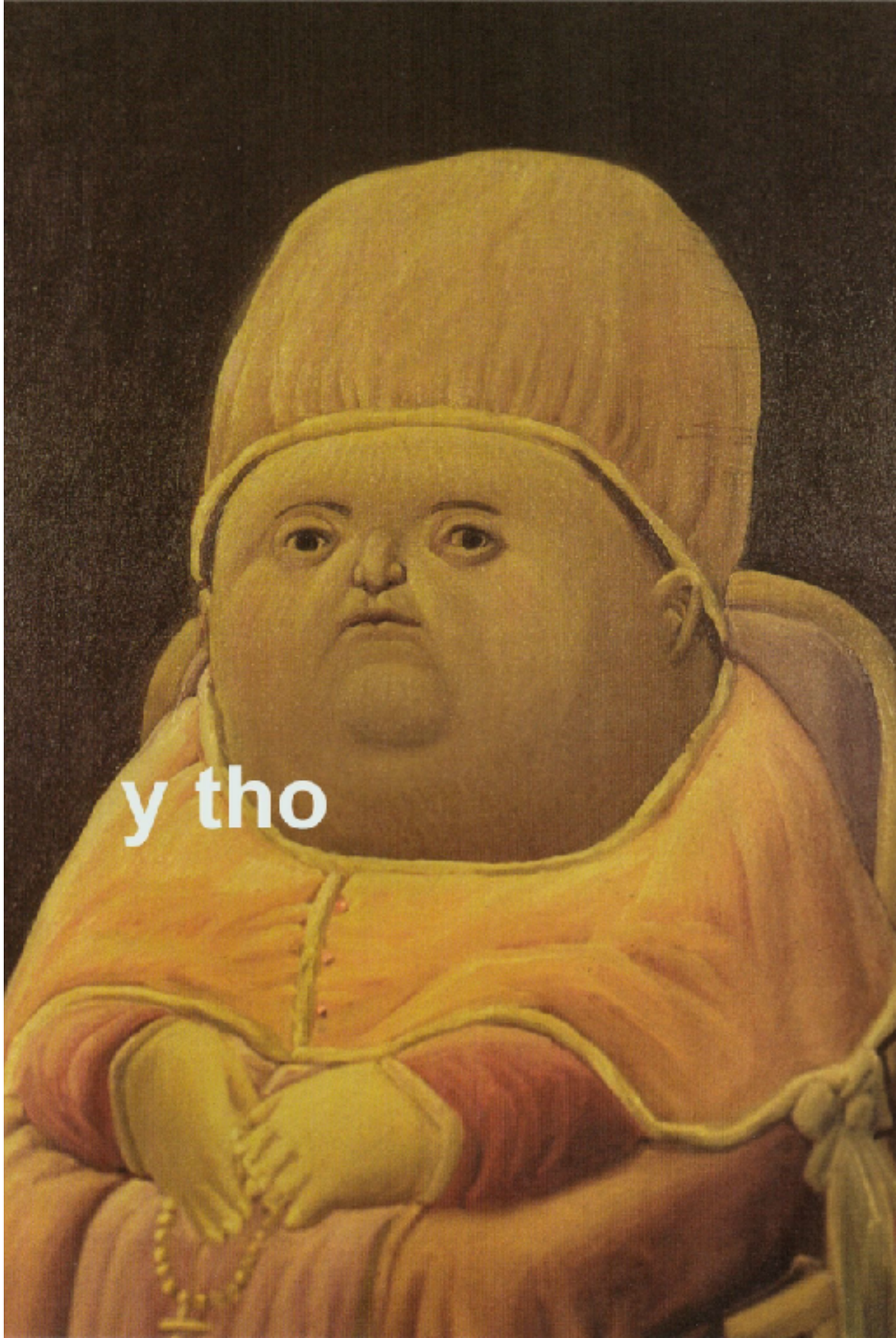

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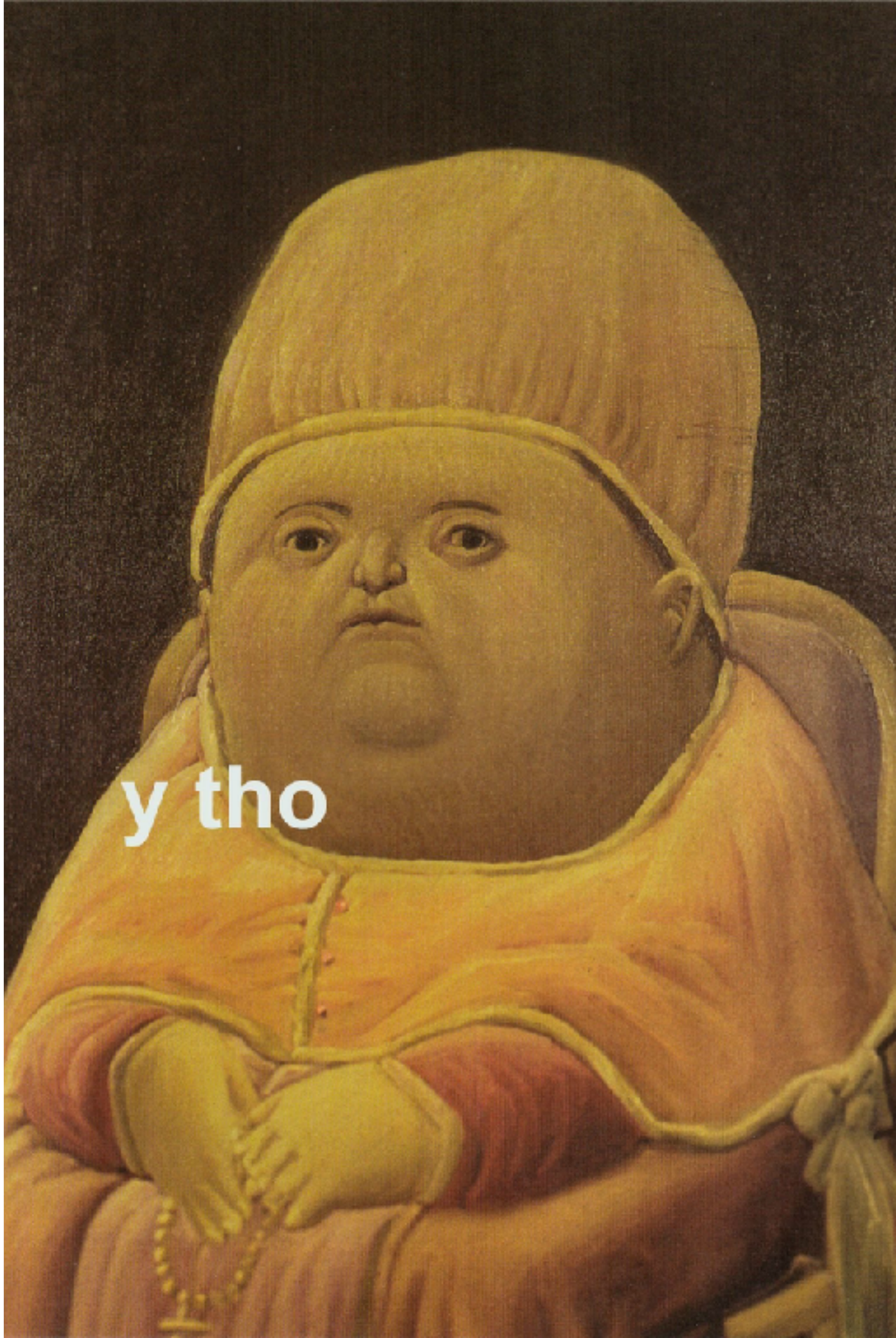

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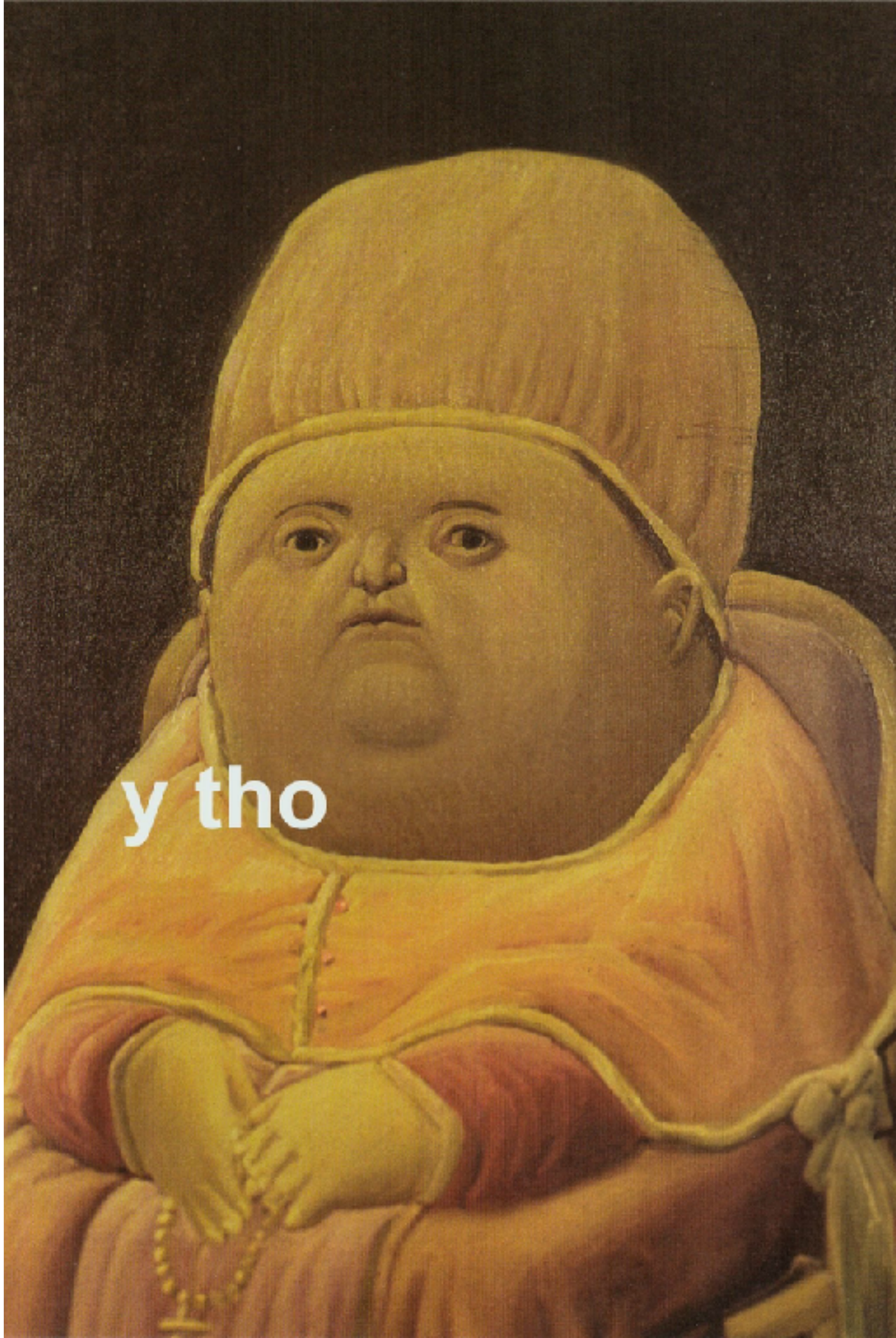

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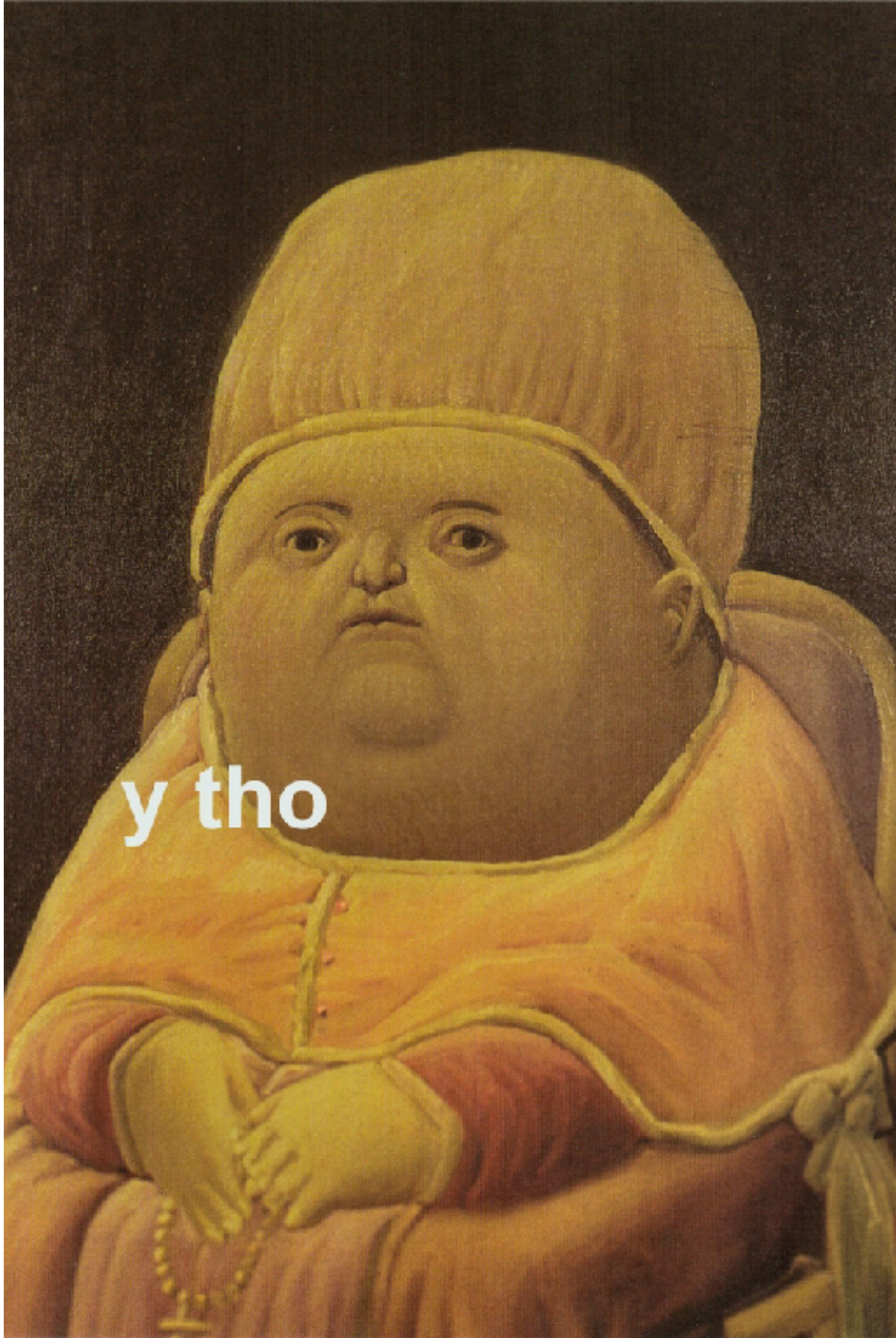

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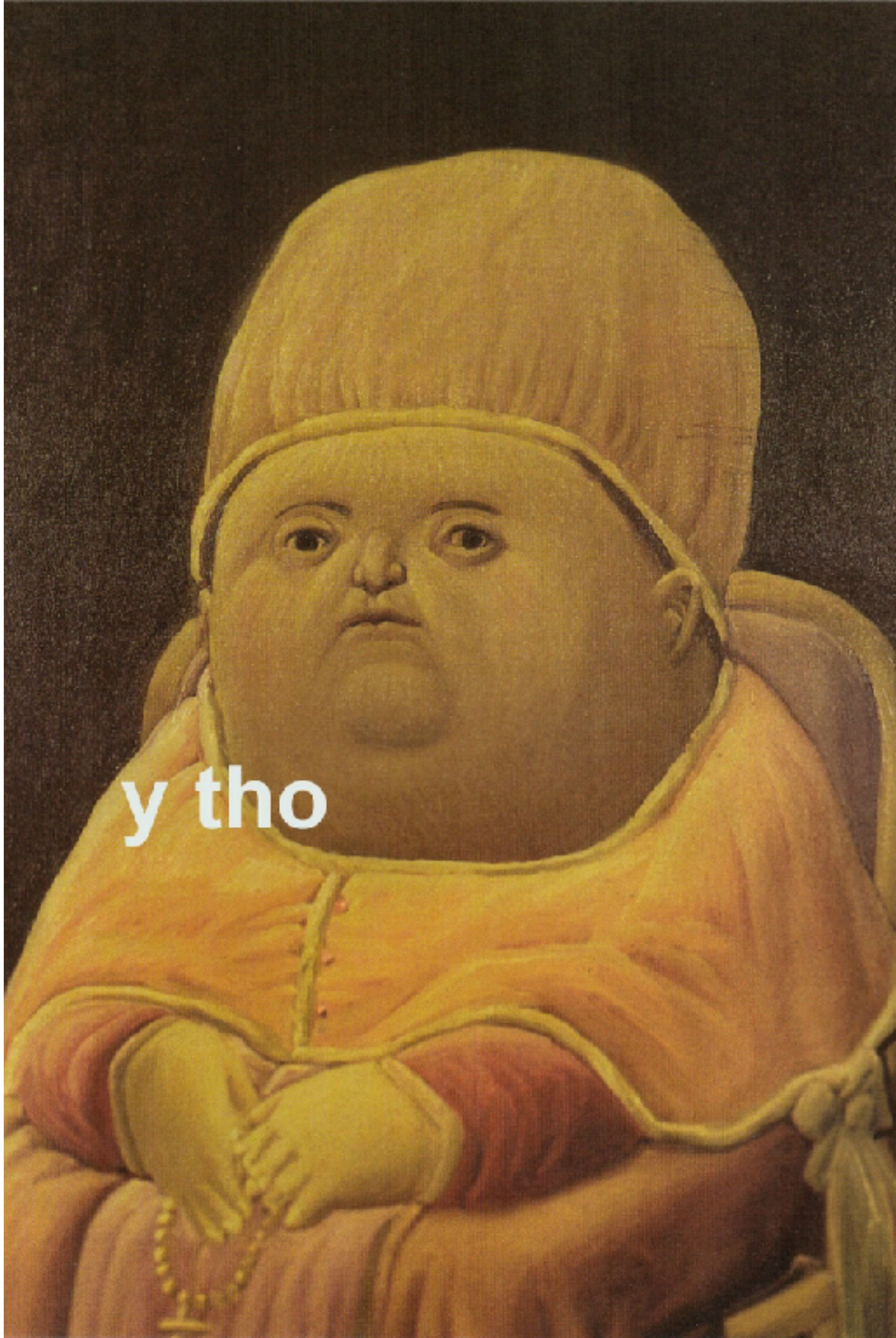

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- Just to know, almost everything *is* modeled with linear algebra